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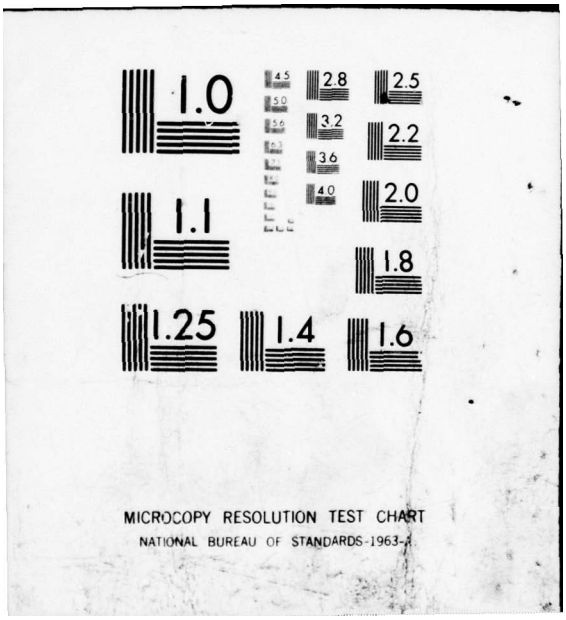
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AFAL-TR-78-185

FIBER OPTICS RECEIVER INTEGRATED CIRCUIT DEVELOPMENT

Ben R. Elmer

Honeywell Inc.
Systems and Research Center
Minneapolis, Minnesota 55413

December 1978

FINAL REPORT

June 1976–July 1978

AIR FORCE AVIONICS LABORATORY
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
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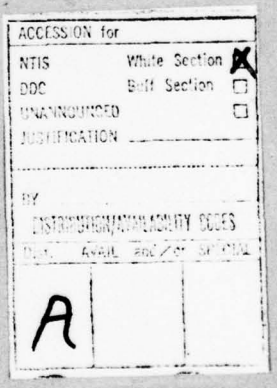

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This report describes the development of the Fiber Optic Receiver Integrated Circuit (FORIC) from synthesis through analysis, layout, processing, packaging, and testing the 1050 parts that were delivered. Detailed test, burn-in, and qualification plans are also included. One of the highlights of this report is an Application Information section, written to inform users of the characteristics of the device that are not apparent from reading the specification.

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PREFACE

This final technical report on the Fiber Optics Receiver Integrated Circuit (FORIC) Development program was submitted by Honeywell Inc., Systems and Research Center, 2600 Ridgway Parkway, Minneapolis, Minnesota 55413, under Contract F33615-76-C-1275 for the U. S. Air Force Avionics Laboratory, Wright-Patterson Air Force Base, Ohio 45433. The AFAL Contract Monitor was Gary Gaugler. The Principal Investigator was Ben R. Elmer; Dave Fulkerson and Greg Schmitz were the other major Honeywell contributors. The author wishes to acknowledge the significant contribution of Dr. J. Robert Biard of Spectronics, who defined the concept and major functions required, as well as detailed design, and contributed many hours of analysis and refinement.

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

TABLE OF CONTENTS (continued)

TABLE OF CONTENTS (concluded)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (continued)

LIST OF ILLUSTRATIONS (concluded)

LIST OF TABLES

SECTION I

INTRODUCTION, SUMMARY, AND RECOMMENDATIONS

INTRODUCTION AND SUMMARY

Fiber optics has an ultimate goal of providing sophisiticated signal transmission systems which take advantage of the wide bandwidth and high interference rejection capabilities of optical data links. This type of information transmission system will be lightweight, small, immune to EMI and EMP, and economical. However, current fiber optic links are hampered by exceedingly high cost components, especially the transmitter and receiver modules, which preclude fiber optics for general use in military systems.

This document constitutes the final technical report of a development program to design, fabricate, test, and deliver approximately 1000 monolithic Fiber Optic Receiver Integrated Circuit (FORIC) devices. The FORICs each contain all functions necessary to amplify photodiode signals. Two active components, a PIN photodiode and the FORIC, are all that is required to convert a light signal from a fiber optic link into a digital transistor-transistor logic (TTL) signal in the range 10 K to 10 M bits/sec.

When properly packaged, these two components will constitute a general purpose receiver module for use in many military applications requiring high reliability, low cost, medium performance characteristics.

This report documents the design process used for the FORIC in addition to describing how it is to be used. The report begins with general capabilities which include some tutorial information that will familiarize the reader with the functions performed by the FORIC. The sensitivity, bandwidth, and dynamic range are briefly described. Specific information on the FORIC device specification and how to use the devices is presented next, followed by a detailed description of the actual circuit operation. The detailed design process is then covered with drawings and equations for obtaining device parameters and determining how they are used in the models that allow computer simulation of the circuit design. Finally, the complete test, burn-in, and qualification plans are presented along with the device packaging information.

RECOMMENDATIONS

There are three major areas that can be addressed to improve the FORIC with minimum risk:

- Packaging
- Yield improvement
- Increased function

Packaging

The TO-100 package (Figure 36) is a very inexpensive, small, reliable, mature semi-conductor package. However, its major disadvantages for packaging the FORIC are the number of leads and the spacing of the leads. Since there are only 10 leads, only one ground can be provided. To properly shield the

input from the output requires at least three ground leads, plus the ability to easily mount shields between the leads as they exit the header. Because of the circular pattern of the 10 leads on a 0.25 inch diameter, shielding is difficult.

A more reasonable packaging approach is to put the FORIC in a leadless chip carrier (LCC). The LCC is really a miniature 14-pin DIP package without a large framework or long leads; shielding is much easier. The LCC costs less than a 14-pin DIP, and it can be mounted on a printed circuit board or a hybrid substrate. Characterization of the FORIC in this type package should reveal improved performance.

Yield Improvement

The original design goal for the sensitivity of the FORIC was 125 nA. During the performance evaluation following the final process runs, a problem in the "on-chip" ground path was discovered. The TTL ground and the pre-amp ground must be connected together, but not on the chip itself. Coupling from output to input results from the present ground path layout on the chip and forces the device specification for sensitivity to be 250 nA. Because of the chip ground path, the lead bonding length and position for both ground and the TTL output are very critical. This results in some loss in packaging yield.

Packaging yield will increase when the chip ground path is corrected. There is also a strong possibility that the sensitivity will improve if this change is made.

Increased Function

The FORIC is intended to be used with Manchester coding. Part of the Manchester decoding function requires information on the status of the input signal to the FORIC. The decoder needs to know if the signal is valid (>250 nA) so it can correct for errors of a given type. The present FORIC does not have a status indicator because at the time of the synthesis of the circuit, no simple method was known. After more exposure to the actual performance of the device and considerable effort devoted to the synthesis of this function, a method of providing a status indicator has been determined. It consists of a differential amplifier, sensing circuit, level translator, current mirror, and TTL open collector output stage. The circuitry required to implement these functions is relatively simple. The area required would not increase the chip size and would have little effect in the overall yield. Because of the difficulty in trying to accomplish the status function external to the FORIC, this internal method is recommended.

SECTION II

GENERAL FUNCTIONAL CAPABILITIES

Figure 1 lists performance characteristics underneath the block diagram of the FORIC.

The primary function of the FORIC is to convert a low level signal current produced by a photon detector into a digital signal. The FORIC's sensitivity and dynamic range combined with its wide data rate range provide the capability required for use in various length point-to-point links. When used with one of a variety of detectors, it provides a general purpose

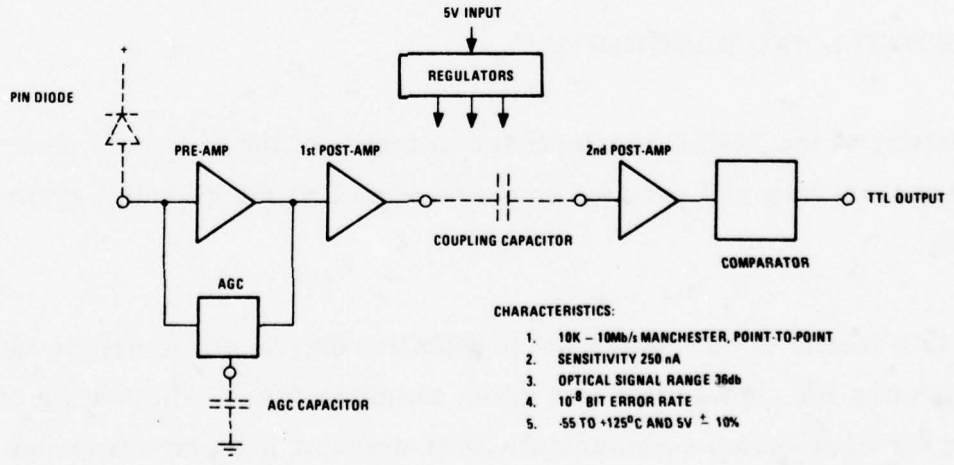

Figure 1. Fiber Optic Receiver Integrated Circuit (FORIC)

optical/electrical conversion interface in a convenient, easy-to-use integrated circuit form.

The FORIC is intended to be used only in point-to-point digital data links. Operation in a data bus environment requires additional circuitry not available on the FORIC. The parameters that describe the receiver performance are:

- Sensitivity and bandwidth
- Dynamic range

The important characteristics of the FORIC are:

- Pre-amp AGC
- AC coupling
- TTL output

A brief discussion of these parameters and characteristics follows.

SENSITIVITY AND BANDWIDTH

Sensitivity of the FORIC is expressed in terms of the minimum peak-to-peak input current that will produce an output signal with a given bit error rate (BER).

BER is a means of estimating the probability that an error will be made in interpreting the signal state at a given sampling time. The source of this error for fiber optics communications is detector and pre-amp noise. The fiber itself does not introduce noise.

The BER is a function of the ratio of the peak signal to the rms noise.[1] Noise is a function of the receiver bandwidth; a larger bandwidth produces more noise. Therefore, to determine the noise amplitude, the detector type, circuit configuration, and receiver bandwidth must be determined. Once the noise is calculated and BER is defined, the minimum signal required to obtain a specified BER at the calculated noise level can be determined. This minimum signal is then the sensitivity; for the FORIC, it is 250 nA peak-to-peak for BER $\leq 10^{-8}$ at a 10 Mb/sec data rate. Another means of expressing sensitivity is to state the minimum input light power to the detector (P_{in}) relative to a reference power (P_{ref} = 1 mW).

$$\text{dBm} = 10 \log \frac{P_{in}}{P_{ref}}$$

For a detector that outputs 0.5 mA/mW, the sensitivity is then -33 dBm for this detector and the FORIC combination receiver.

DYNAMIC RANGE

The dynamic range is usually expressed in decibels and relates the maximum input signal to the minimum input signal. When the input current into the FORIC is used as the input signal, the dynamic range is in electrical decibels.

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[1] J. R. Biard, "Optoelectronic Aspects of Avionic Systems," Final Technical Report AFAL-TR-73-164, April 1973.

$$\text{dynamic range} = 20 \log \frac{I_{max}}{I_{min}} = 20 \log \frac{1000\,\mu A}{250\ nA} = 72\ \text{dB electrical}$$

This can also be expressed in terms of the range of power (light) into the detector. The term "dynamic range" is inappropriate in describing this power expression. Instead, it is usually referred to as the optical signal range (OSR) and is defined as

$$\text{OSR} = 10 \log \frac{P_{in_{max}}}{P_{in_{min}}} = 36\ \text{dB power}$$

This large range (4000:1) is a direct result of the unique pre-amp AGC circuit designed for this IC.

PRE-AMP AGC

As illustrated in Figure 1, the automatic gain control (AGC) for the FORIC operates on the pre-amp itself to extend the OSR beyond the normal range obtainable with the limitations placed on the pre-amp. Given a 5 V TTL compatible power supply, the specified sensitivity necessitates that the FORIC be AC coupled. A bipolar signal (one that swings an equal amount above and below a DC bias voltage) must be developed to transfer the signal across the coupling capacitor. A full 5 V cannot be used for this swing because its tolerance ($\pm$0.5 V) is too large. Therefore, a 3.9 V, "on-chip" regulated supply is used as the supply voltage.

All these considerations limit the dynamic range of the linear pre-amp to 46 dB. The AGC circuit absorbs the excess signal above 46 dB and limits the pre-amp gain to operation within this linear range of 46 dB.

AC COUPLING

One factor that can limit sensitivity of a pre-amp is the drift associated with temperature and/or supply variations. Depending on the particular temperature compensation scheme used, the drift of a pre-amp can be significantly larger than the input noise. If a pre-amp is DC coupled to a post-amp, this drift seriously affects receiver sensitivity.

For optimum performance a DC coupled receiver threshold, the dividing line between a one and zero, should be set just above the noise with no input signal present. Since drift affects the threshold, it is necessary to increase the threshold-to-noise separation by the maximum expected drift. This increases the required input signal for most operating conditions. The FORIC is AC coupled as indicated in Figure 1.

AC coupling improves sensitivity over DC coupling for a large temperature range, but AC coupling confines the input signal to a constant average value for all time intervals comparable to the AGC time constant. NRZ coding with long strings of 1's or 0's cannot be, for example, reproduced across the coupling capacitor. An encoding scheme such as Manchester,[2] which

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[2] J. R. Biard, "Optoelectronics Aspects of Avionics Systems II," Technical Report AFAL-TR-45, May 1975.

has a transition in every bit time to keep the average value of the signal constant, must be used.

TTL OUTPUT

The post-amp output of the FORIC is a bipolar signal of relatively large amplitude referenced to the 3.9 V internal supply. However, this type of signal does not meet the requirements for the FORIC output. A comparator stage consisting of cross coupled current sources referenced to ground is used to translate this signal down to a ground referenced signal that is fed into a TTL output stage. The output is compatible with the 5400 series TTL logic family.

SECTION III

APPLICATION INFORMATION

The FORIC is intended to be used as a general purpose receiver for fiber optic point-to-point links. It can interface with PIN photodiodes or avalanche photodiodes of various types. The main advantages of the FORIC over hybrid or discrete implementations are:

- No adjustments (trim pots, etc.) required
- Small physical size
- Higher reliability (fewer connections)
- Lower production cost

Because the FORIC is a monolithic integrated circuit, it has the features that make it easy to use in general purpose applications.

The information required to apply the FORIC in a point-to-point link is detailed in this section. The section begins with a formal device specification and then treats various functional and physical details of the FORIC.

DEVICE SPECIFICATION

Electrical Characteristics

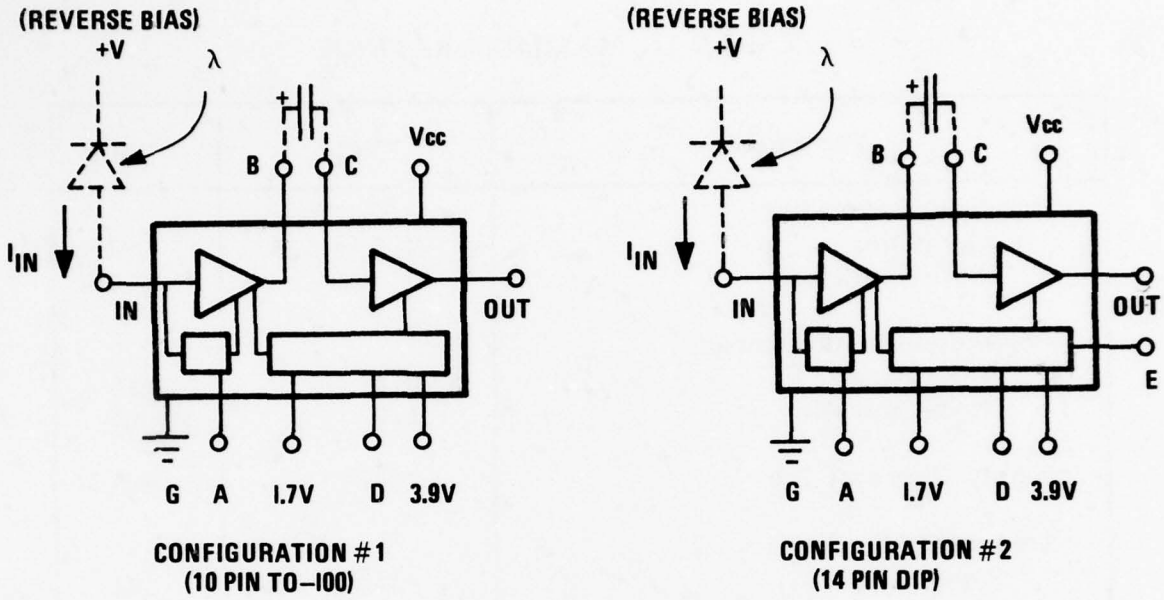
The performance characteristics apply over the operating temperature range and supply voltage listed in Table 1 (-55°C to +125°C, +5 V $\pm$ 10 percent). The IC operates as depicted in Figure 2 and has the following characteristics:

DC Performance Characteristics--

- Maximum Ratings:
  The maximum ratings are as specified in Table 1.
- Supply Voltage and Current:
  The IC supply voltages are ground and +5 V $\pm$ 10 percent, and the supply current will not exceed 70 mA under all operating conditions.
- Input Characteristics:
  The input characteristics are specified in Table 2.
- Output Characteristics:
  The output characteristics are as specified in Table 3. The output load should be one standard 5400 series TTL input.

TABLE 1. MAXIMUM RATINGS

Parameter	Value	Units
Supply Voltage, Vcc		
Operating	4.5 to 5.5	Volts
Non-Operating	7	Volts
Photodiode Input Current		
Operating	0.5	mA
Non-Operating	1.0	mA
Supply Current, Icc	70	mA
Temperature		
Operating	-55 to +125	° C
Non-Operating	-65 to +150	° C
Device Junction Temperature, Tj	+150	° C
Power Dissipation, Pd	400	mW
Lead Temperature (soldering 10 sec)	250	° C



FOR PIN NUMBERS, SEE FIGURE 7

IN	=	PHOTODIODE CURRENT INPUT
OUT	=	TTL OUTPUT
Vcc	=	SUPPLY VOLTAGE
G	=	SUPPLY REFERENCE
A	=	AUTOMATIC GAIN CONTROL (AGC)
B	=	PREAMP OUTPUT
C	=	OUTPUT STAGE INPUT
D	=	3.9V FILTER POINT
1.7V	=	1.7V REGULATOR OUTPUT
3.9V	=	3.9V REGULATOR OUTPUT
E	=	BAND GAP REGULATOR OUTPUT

Figure 2. FORIC Package Options

TABLE 2. INPUT CHARACTERISTICS

Parameter	Test Conditions	Min	Typ	Max	Unit
Non-Operating Photodiode Input Current		-	-	1	mA
Total External Input Capacitance	Note 1	-	-	3.0	pF

Note 1: All parasitic (leads, sockets, etc.) plus the photodiode capacitance is included in this condition.

TABLE 3. OUTPUT CHARACTERISTICS

Parameter	Test Conditions	Min	Max	Unit
High Level Output Voltage V_{OH}	Vcc = 4.5 V	2.4		V
High Level Output Current I_{OH}	Note 1, V_{OH} = 2.4 V		400	μA
Low Level Output Voltage VOL	Vcc = 5.5 V I_{OL} = -16 mA Note 1		0.4	V
Low Level Output Current I_{OL}	Vcc = 4.5 V, Note 1		-16.0	mA
Short Circuit Output Current	V_{OH} = 2.4 V min. before shorting, Note 1		-55	mA

Note 1: Measured over operating temperature and supply range.

AC Performance Characteristics--

- Switching Characteristics:
  The switching characteristics from the input current to the output voltage are in accordance with Table 4 and Figures 3, 4 and 5. The allowable data rate of the IC is between 10 K and 10 M bits/sec (Manchester).

Environmental Conditions

The FORIC is processed to meet MIL-STD-883B testing for class B parts.

Unpackaged Chips--The unpackaged chips pass MIL-STD-883B internal visual (monolithic) test--Method 2010.2, Condition B.

Packaged Units--The packaged units pass MIL-STD-883B as shown in Table 5.

PACKAGE PIN OUT INFORMATION

The FORIC was delivered in three configurations: unpackaged "chips," 14-pin ceramic DIPS, and 10-pin TO-100 cans. The unpackaged chips can be used on hybrid substrate assemblies or in "leadless" chip carriers. Figure 6 is a photomicrograph of the unpackaged chip showing the relative pad (connection points) positions. These chips are DC tested and visually inspected only. No AC testing or hermetic sealing is possible for the chips in this configuration.

TABLE 4. SWITCHING CHARACTERISTICS

Parameter	Min	Typ	Max	Units
Data rate (DR) Manchester coded data (see Figure 4)	10^4		10^7	bits/sec
Photodiode current input I_I Including dark leakage current I_{DD} and signal current (see Figure 4)	0.250		500	μA
Bit error rate $I_I \geq 250$ nA $10^4 \leq DR \leq 10^7$ bits/sec			10^{-8}	error/sec
Input transition time High-to-low and low-to-high $T_{I_{HL}}$ and $T_{I_{LH}}$			15	nsec
Input pulse width T_1 or T_2 $T_1 + T_2$ (see Figure 3)	40 0.1		 100	nsec μsec
Output pulse width T_3 T_4 (see Figure 3)	T_1-7 T_2-7	T_2 T_2	T_2+7 T_2+7	nsec nsec
Delay time low-to-high $T_{D_{LH}}$		30	75	nsec
Delay time high-to-low $T_{D_{HL}}$		30	75	nsec
Output transition time Low-to-high $T_{O_{LH}}$	3	7	15	nsec
Output transition time High-to-low $T_{O_{HL}}$	2	4	15	nsec

Note: All switching characteristics are measured with the standard load shown in Figure 4.

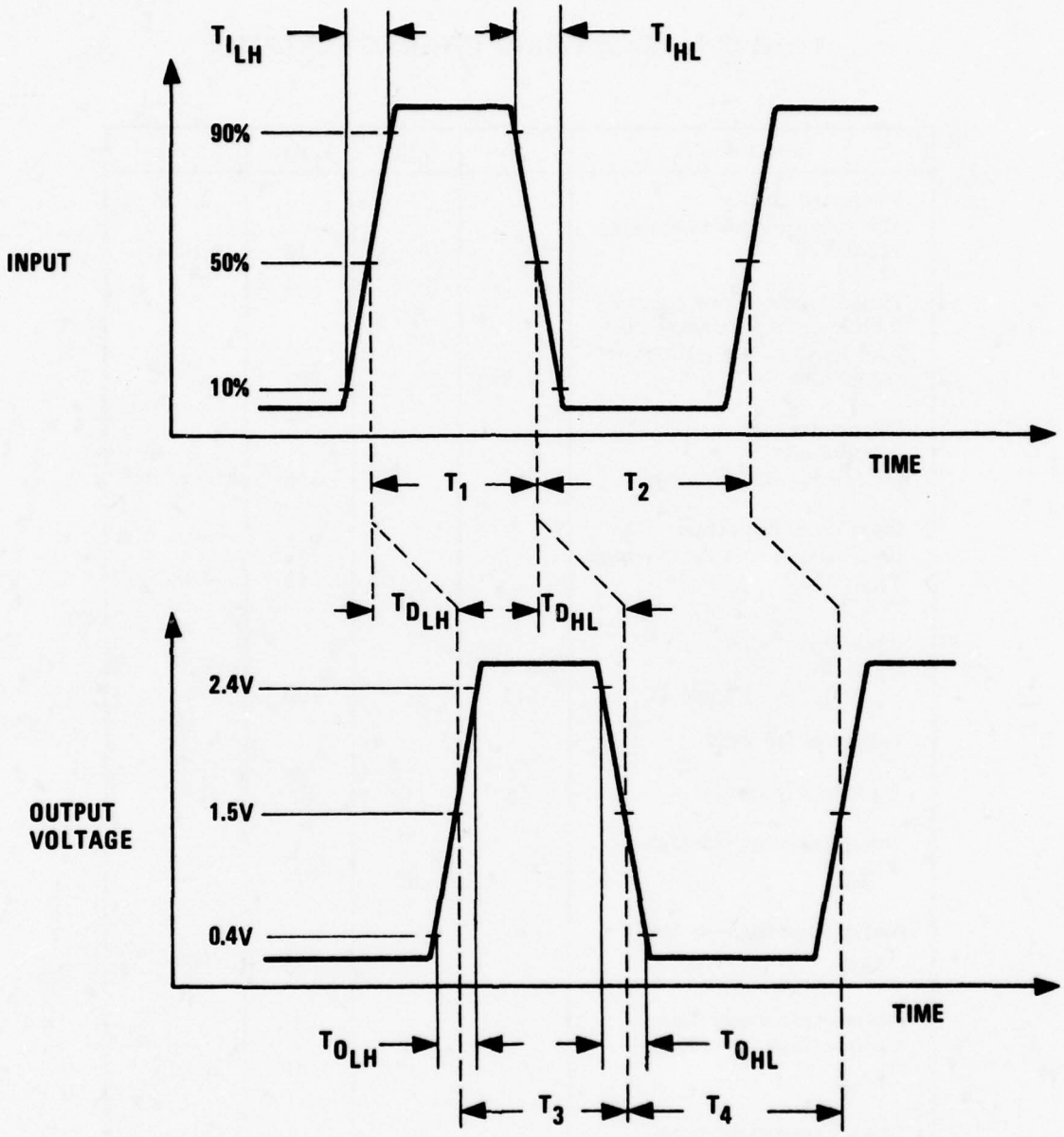


Figure 3. Receiver Input/Output Risetime Definitions

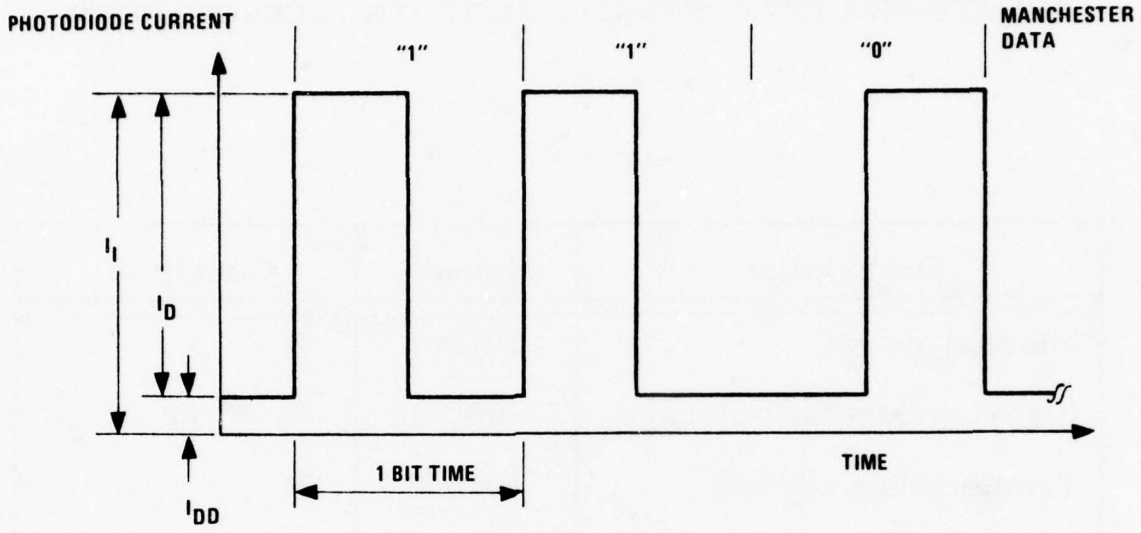


Figure 4. Manchester Code

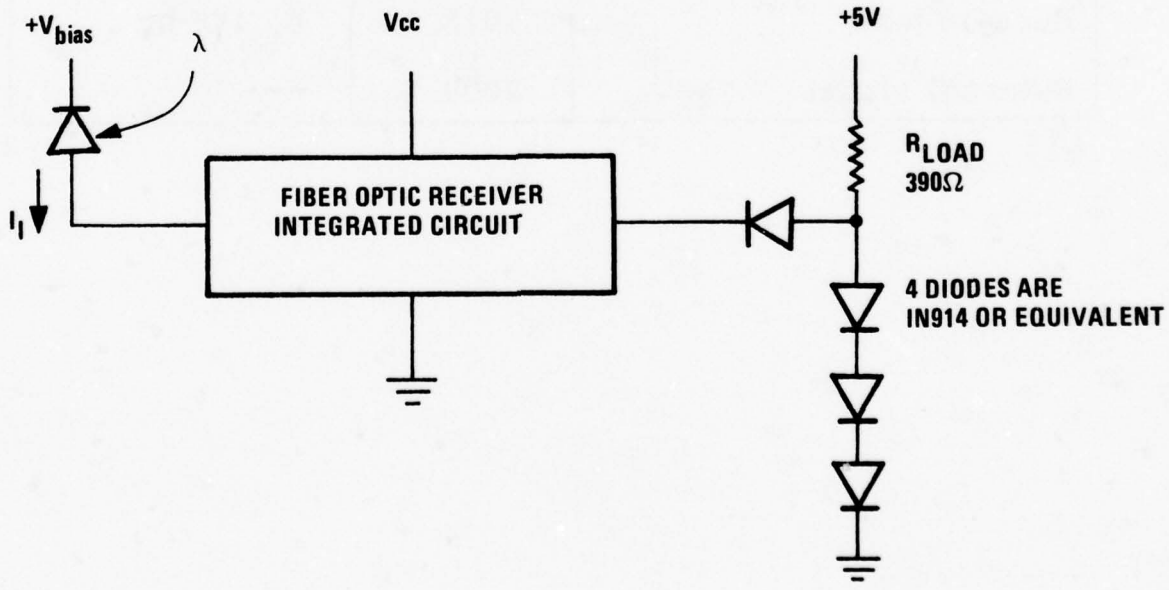


Figure 5. Output Equivalent Circuit for One TTL Load

TABLE 5.
MIL-STD-883A ENVIRONMENTAL TESTS FOR PACKAGED UNITS

Description	Method	Condition
Internal visual	2010.1	B
High-temperature storage	1008.1	C, 24 hr
Temperature cycling	1010.0	B
Constant acceleration	2001.1	E, Y, axis only
Fine and gross leak	1014.1	---
Burn-in test	1015.1	B, 168 hr
External visual	2009.1	---

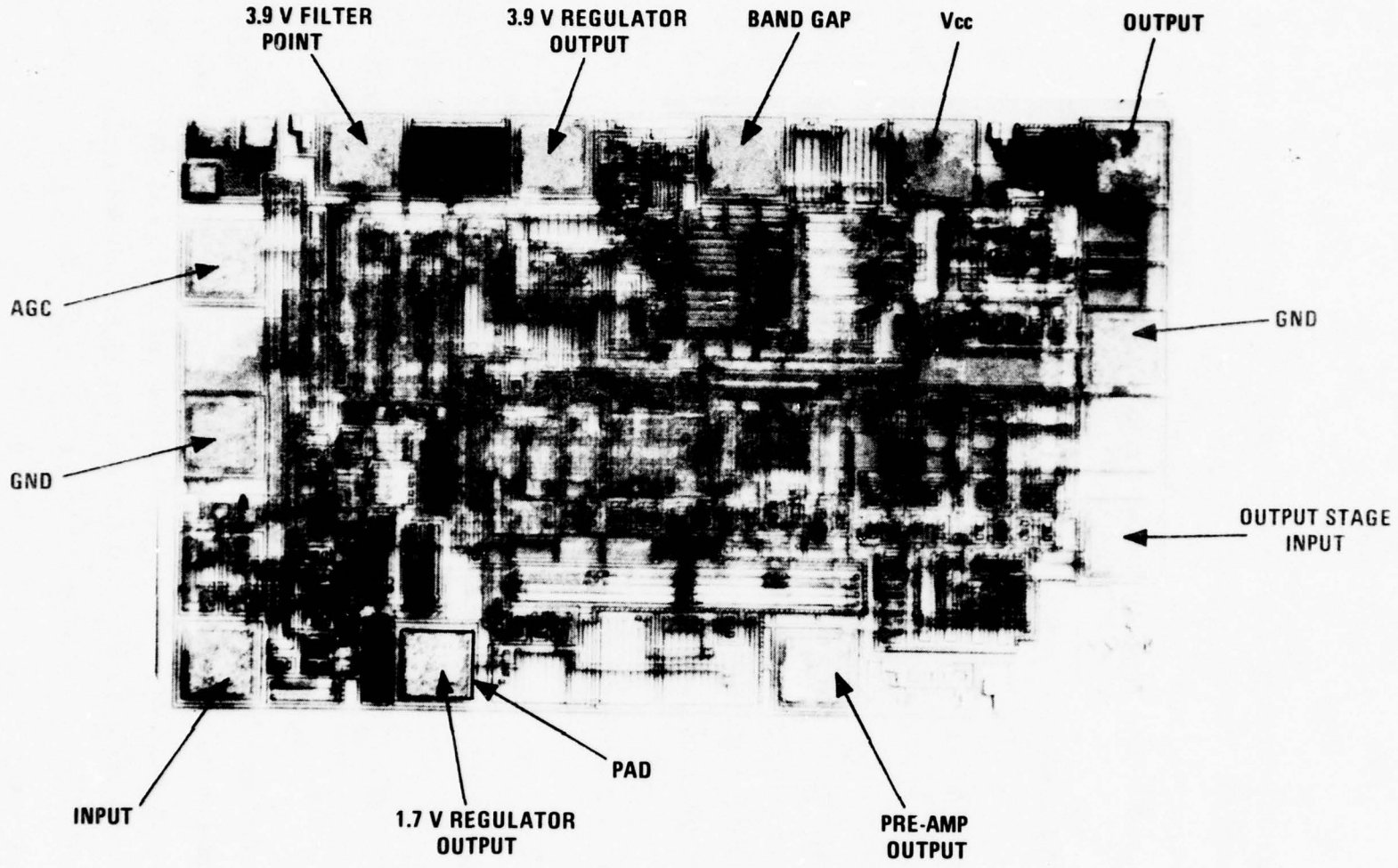


Figure 6. Photomicrograph of FORIC

Figure 7 shows the pin connection diagrams for both 14-pin DIP and TO-100 packages. The pin labelled NC indicates no internal connection is made to that package pin; thus, it can be used as a tie point or grounded. These packaged chips are fully tested and hermetically sealed.

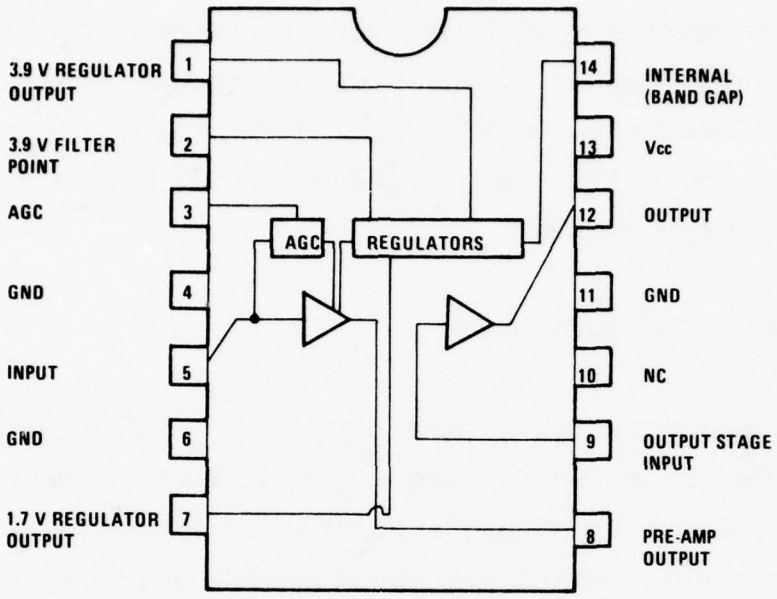
POWER SUPPLY FILTERING

Filtering the V_{cc} supply as close to the FORIC V_{cc} pin as possible is necessary to provide a clean output current waveform. Both high and low frequency filter capacitors are required because of the extremely low level input signals being sensed. Filter capacitor values are dependent on the power supply used, but a 4.7 μF in parallel with a 0.1 μF capacitor will be adequate for most power supplies. Short leads on the capacitors combined with a ground plane are recommended.

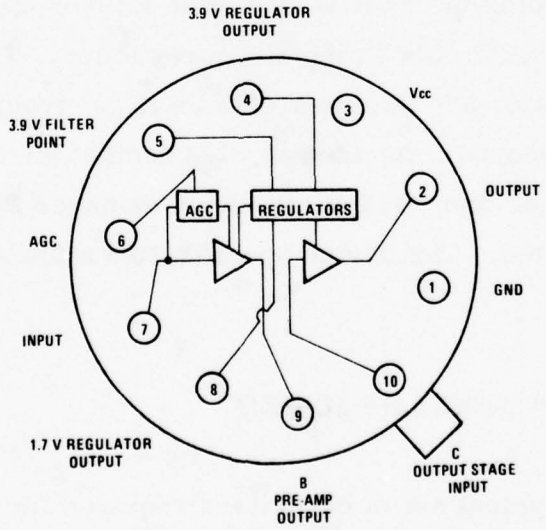
PHOTODIODE TYPE AND FILTERING

The FORIC is compatible with a number of photodiodes. However, certain types of photodiodes with anodes tied to the case are not recommended for use with the FORIC. Difficulties in shielding the case of this type of photodiode from EMI and the large capacitance associated with the case tend to limit the FORIC sensitivity.

Various bias voltages from 5 V to 90 V are required by the different types of photodiodes. Whatever the bias voltage, some filtering is required to prevent extraneous signals from getting into the photodiode. In addition, adding a photodiode current limiting resistor is recommended. The filtering arrangement chosen depends on the supply used but a 1 KΩ series resistor



a) 14-Pin Ceramic DIP



b) 10-Pin TO-100

Figure 7. Pin Connection Diagrams for the 14-Pin Ceramic DIP and 10-Pin TO-100 Packaging Configurations

with a 0.1 μF capacitor is adequate to limit the current and filter most bias supplies. An important point is that the 1.7 V regulator output is actually "signal ground" as far as the FORIC input is concerned. Therefore, any filter capacitor on the bias supply should be returned to the 1.7 V regulator pin instead of supply ground.

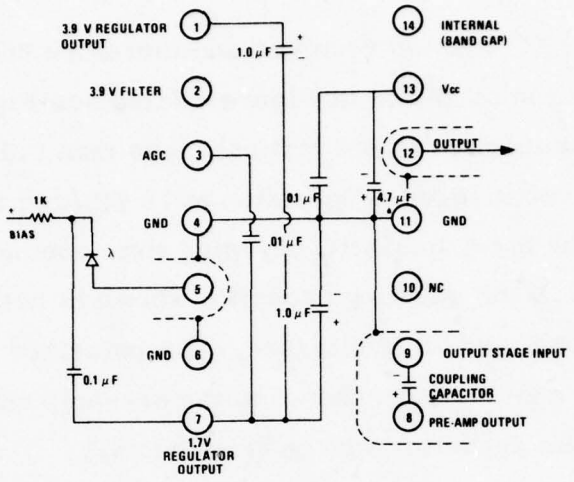
FORIC INPUT CONSIDERATIONS

The DC bias point of the FORIC input is +1.7 V, and it is a current sink. This means that the photodiode anode must be connected to the input pin and that the reverse bias supply must be positive with respect to the +1.7 V supply. As mentioned before, the "signal ground" relative to this input is the 1.7 V regulator output.

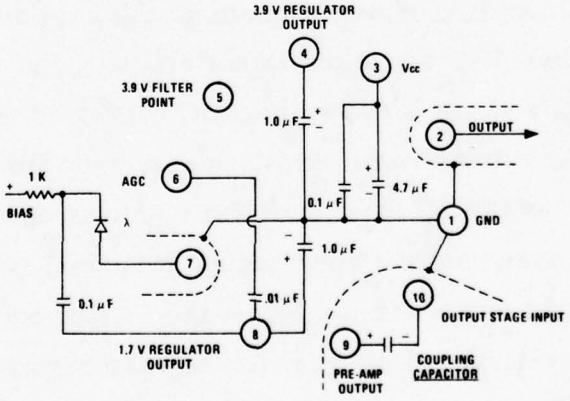
Accidentally grounding the FORIC input will not damage it, but it will cause approximately 25 mA to flow in the 1.7 V regulator. This current may overheat the regulator and lead to problems if the grounding remains for more than a few seconds. Accidentally connecting the input to the Vcc or other voltage greater than +1.7 V can cause damaged input circuitry if the current is not limited. The device specification allows 1 mA maximum input current.

EXTERNAL COMPONENTS REQUIRED

Figure 8 shows a typical set of capacitors required for normal operation of the FORIC with a Manchester codes (constant average value) input signal. In addition to those capacitors for power supply and photodiode bias supply filtering, certain other capacitors are required.



a. 14-Pin DIP



b. 10-Pin TO-100

Figure 8. External Component Values and Connections

Coupling Capacitor

The FORIC is an AC coupled receiver and therefore requires a coupling capacitor connection as shown in Figure 8 (also see Figure 1). Although the value of this capacitor is not critical, less than 0.1 μF or greater than 100 μF is not recommended. Operation at 10 Mb/sec requires a small value coupling capacitor for a small RC charging time compared with a 10 Kb/sec data rate. The 1.0 μF coupling capacitor shown is used for testing FORIC devices at both 10 K and 10 M bits/sec. If a polarized capacitor is used, the positive side should be connected to the pre-amp output. The maximum voltage across this capacitor will be less than 5 V.

AGC Capacitor

The AGC capacitor maintains a voltage proportional to the average input signal swing, which in turn essentially controls the gain of the pre-amp. The actual value of this AGC capacitor is not critical, but a range of 0.001 to 10 μF is recommended. A large value AGC capacitor will take a long time to reach its final voltage value; thus, the start-up time from first putting a signal into the FORIC input until valid data is obtained on the FORIC is long. However, once it has reached this final value, small variations in average signal value will not affect the FORIC output. A small value AGC capacitor will have a short start-up time but may be sensitive to input data average value changes. The 0.01 μF AGC capacitor shown in Figure 8 is adequate for normal signals. This AGC capacitor is physically connected between the AGC pin and the +1.7 V regulator output because the 1.7 V regulated output is the "signal ground."

Regulator Filter Capacitor

Both the 1.7 V and the 3.9 V regulator outputs require external filter capacitors. Although Vcc is adequately filtered as mentioned above, the "on-chip" regulators experience small output variations caused by the signal and/or on-chip noise sources. Satisfactory performance has been obtained with the 1.0 μF capacitors shown in Figure 8. The 3.9 V capacitor must be connected to the 1.7 V output and its capacitor is connected to ground.

PHYSICAL MOUNTING CONSIDERATIONS

Because of the very sensitive FORIC input and very large swing TTL output, some precautions in physical placement of components is required.

The most important physical mounting consideration is the proper routing of the photodiode to FORIC input wiring. There are two opposing considerations that must be mediated to obtain proper circuit operation. First, the input capacitance to ground must be minimized. The device specification allows 3.0 pF maximum. Second, the coupling capacitance between the input and any other noise or signal source must be minimized. For example, a 5 ns fall time of the 3 V TTL output (1.3 V change relative to +1.7 V input bias) can couple a 250 nA pulse into the input with one femtofarad (1 x 10^{-15} F) coupling capacitance. That pulse would be equal to the normal signal amplitude.

The ideal shielding scheme would surround all components, leaving the input unshielded. That scheme would minimize both coupling capacitance and

capacitance to ground from the input. This ideal scheme is not completely realizable, but can be approximated by:

1. Minimizing the lead length from photodiode to FORIC input. (The FORIC test fixture has a 0.25 inch length.)
2. Shielding the input from all its surroundings but minimizing capacitance to the shield from the input by keeping the spacing to greater than 0.1 inch.

Other components that require care in mounting position are the AGC capacitor and the coupling capacitor. Although these capacitors are not as sensitive to picking up extraneous signals as the FORIC input is, neither component should be placed close to the output. The connection lengths to these components should also be minimized to minimize coupling to the output.

Any connection to the 3.9 V filter point or the internal (band gap) point should be avoided to minimize coupling to the output. These points were made available for testing purposes only.

The mounting of the TO-100 package requires a special connection between the metal can and ground in addition to the above precautions. Specifically, the small tab that indicates pin 10 (see Figure 7) plus a point on the can opposite pin 10 must both be grounded with a minimum length lead. Use of this package configuration is not recommended because of the difficulty in properly shielding the input from the output.

SECTION IV

CIRCUIT DESCRIPTION

The FORIC is a very sensitive, wide band, AC coupled linear amplifier with a large dynamic range and a digital TTL output. The digital output serves only as a standard interface buffer that "squares up" the signal. The FORIC is comprised of six major circuits:

- Pre-amp with AGC
- Post-amplifiers
- Output stages
- Band gap regulator
- 3.9 V regulator
- 1.7 V regulator

The complete schematic of all these circuits interconnected is shown in Figure 9.

PRE-AMP WITH AGC

The pre-amp portion of the FORIC is shown in block diagram form in Figure 10. This circuit consists of a differential amplifier, a DC feedback loop and current source to stabilize the bias conditions, an averaging (AGC) capacitor in a feedback loop to control the pre-amp transresistance (AGC circuit), and voltage followers to isolate these loops from the first post-amp stage.

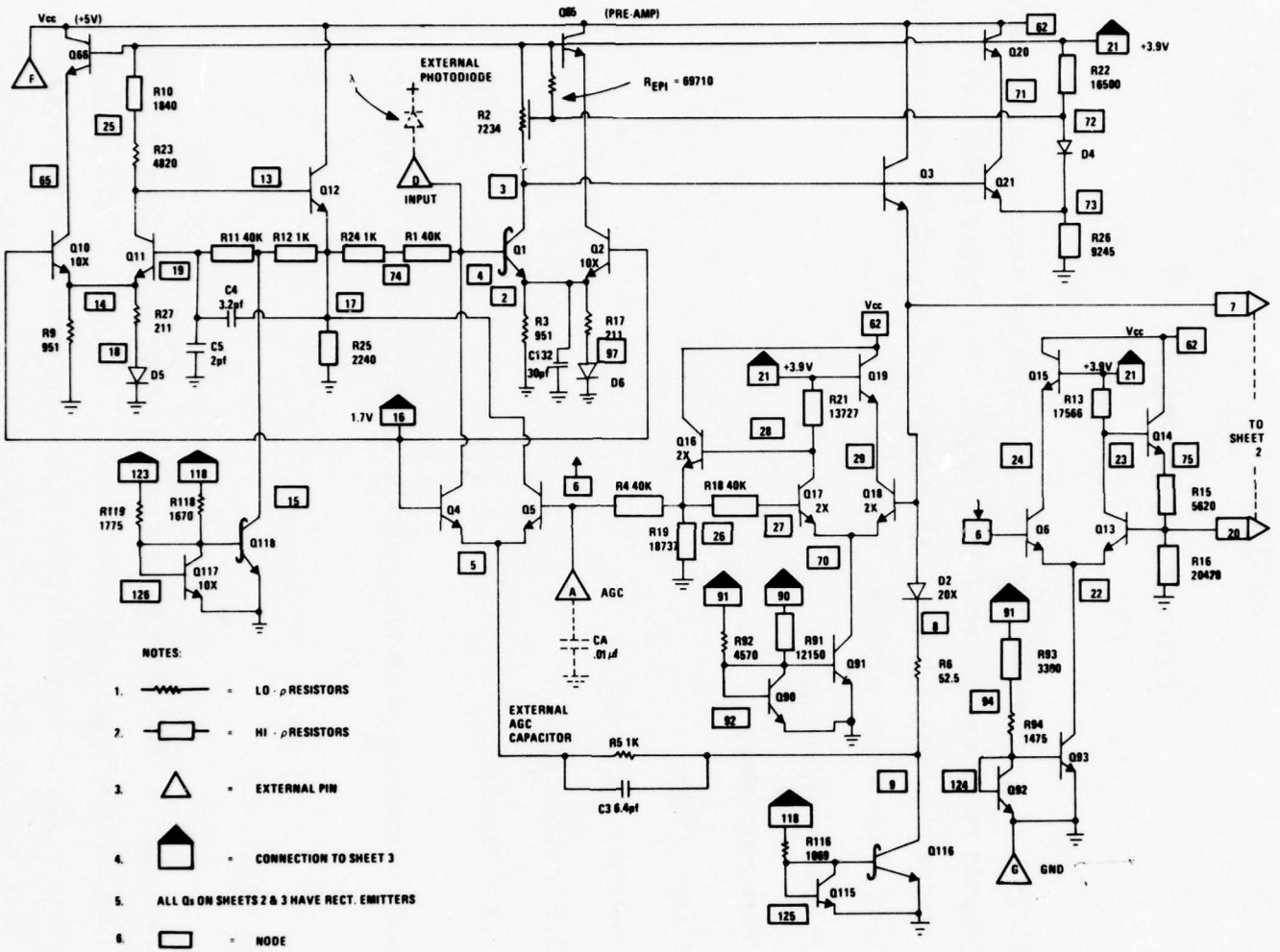


Figure 9. Schematic of Fiber Optic Receiver Integrated Circuit

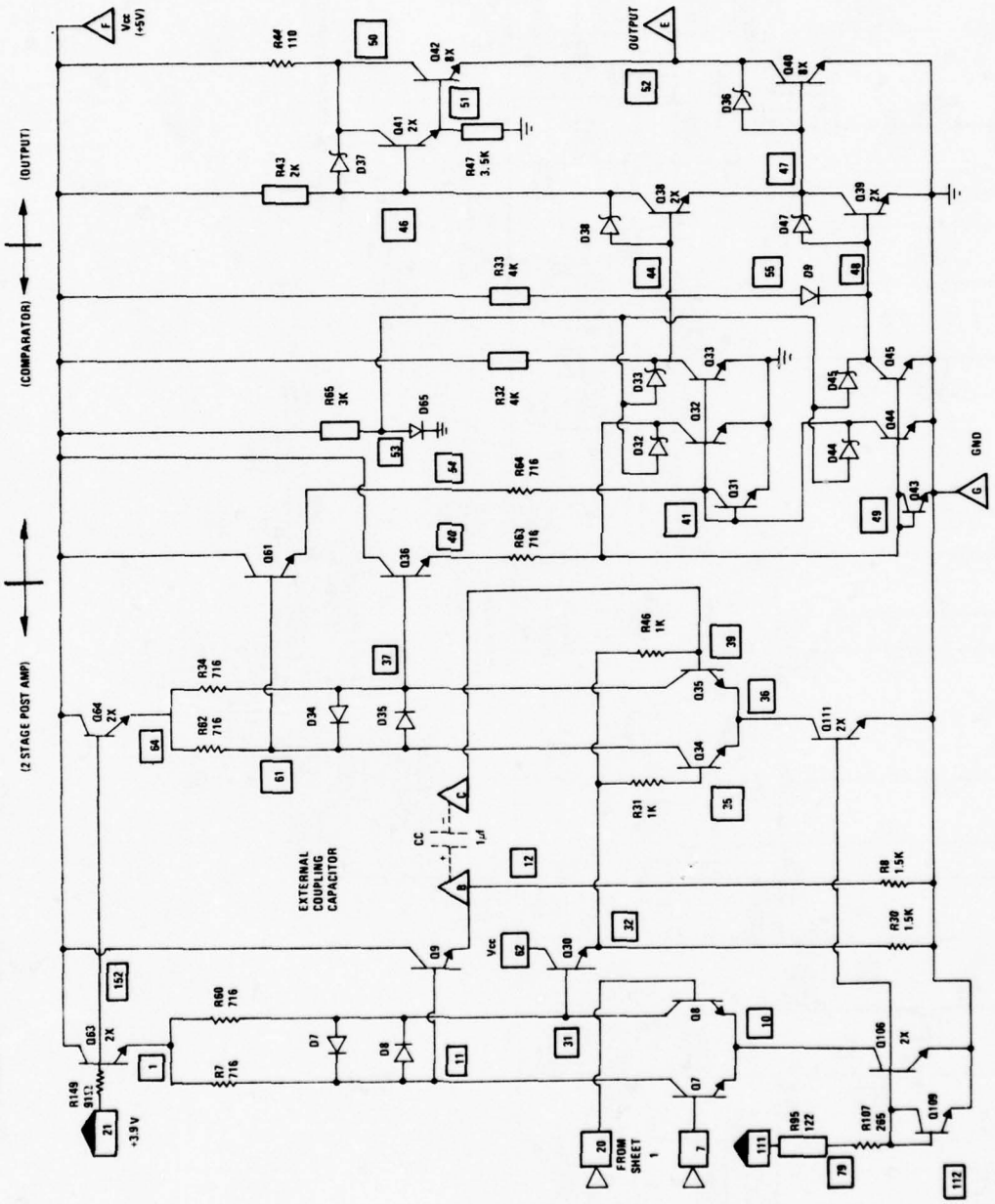


Figure 9. Schematic of Fiber Optic Receiver Integrated Circuit (continued)

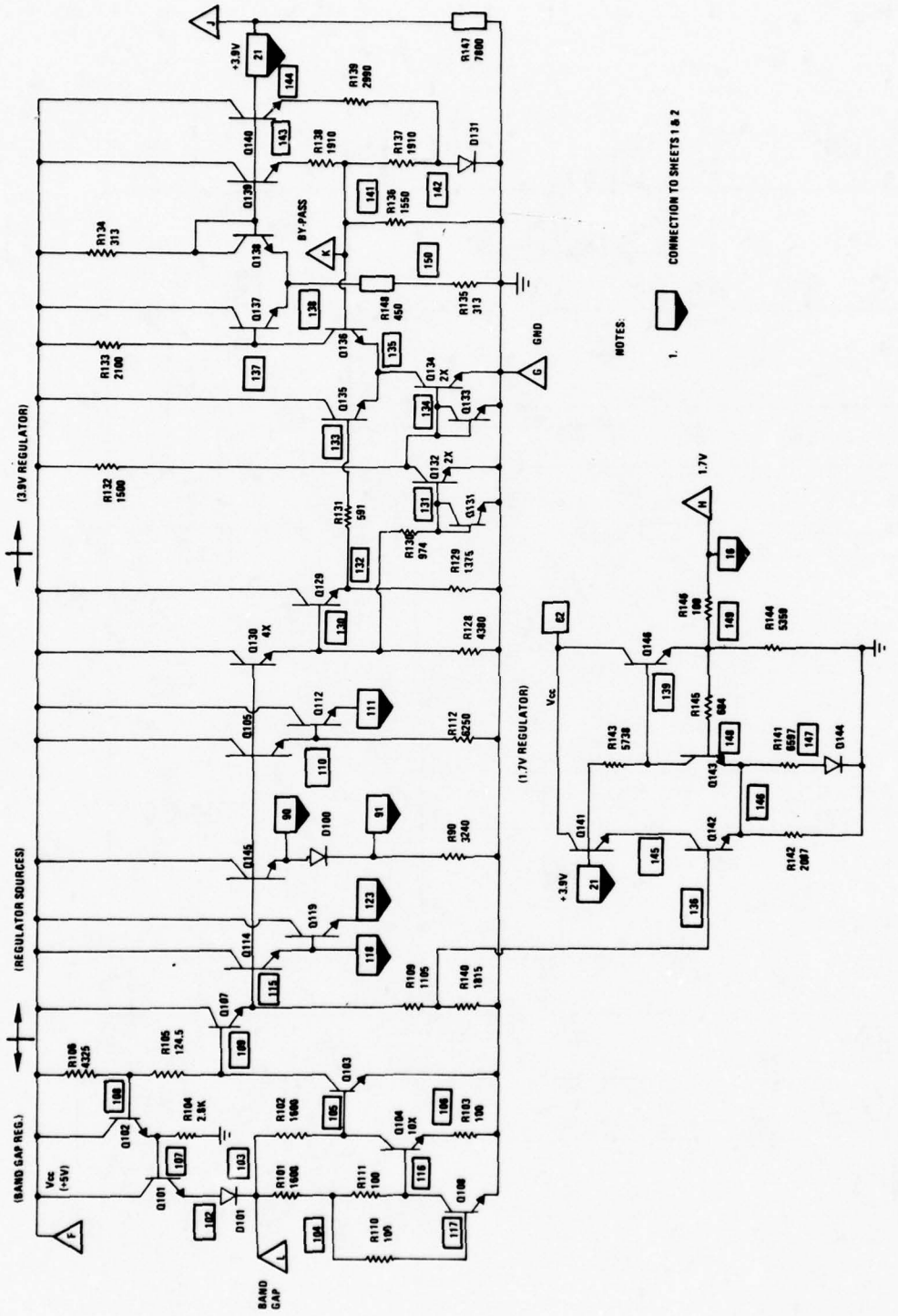


Figure 9. Schematic of Fiber Optic Receiver Integrated Circuit (concluded)

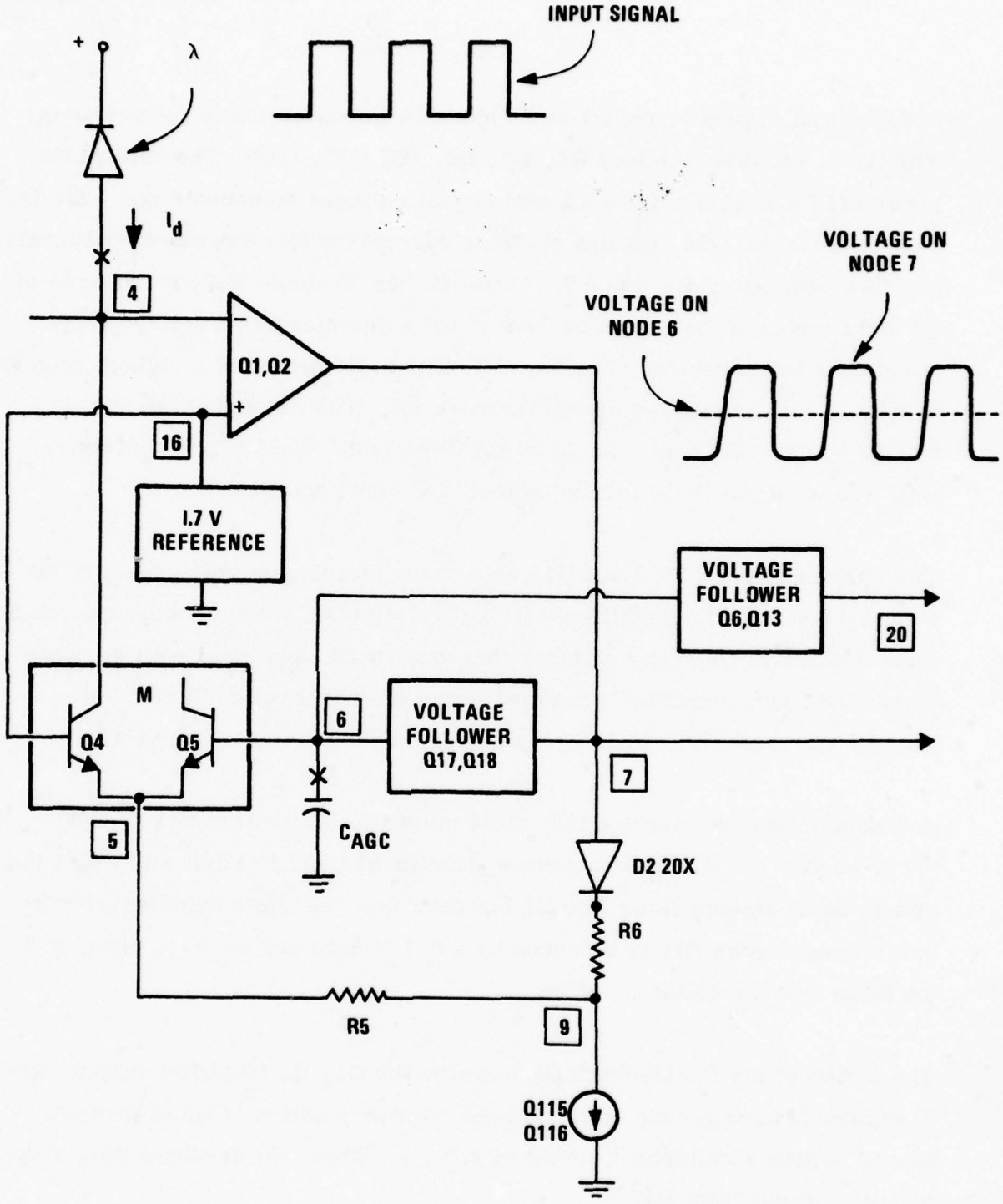


Figure 10. Block Diagram of FORIC Pre-Amp

Referring to Figure 9, page 1 and Figure 10 for operation of the pre-amp with AGC, consider the loop Q5, R5, R6, D2, Q17, Q18. The voltage follower (Q17 and Q18) acts to maintain equal voltages on nodes 6 and 7 for DC bias conditions. Q16 supplies the base current for Q5; therefore no current can flow between nodes 6 and 7. Diode D2 has 20 times the emitter area of Q5 and carries 20 times the current (1 mA); therefore, the voltage drops track over temperature. The 1 mA flowing in R6 produces a voltage drop of 0.0525 V; this same drop appears across R5. The current in R5 is then 0.0525 V/1 K = 52.5 μA. Since 50 μA flows in Q5 (1/20 of the current in D2), 2.5 μA flows in Q4 for "no signal" DC bias conditions.

The voltage follower Q10 and Q11 acts to maintain equal voltages on nodes 16 and 4 (the input). Amplifiers Q10, Q11, and Q1, Q2 have their DC conditions duplicated in such a manner that they track each other over temperature. Q10, Q11 amplifier's frequency response is down 3 dB at 1 MHz because of C4 and C5 and doesn't interfere with Q1, Q2 AC performance.

A constant current source Q117, Q118 pulls 100 μA through R12 to drop 0.1 V across it. Additional current through R12 and R11 flows into Q11 base and an equal amount flows into Q1 because both are biased similarly. The 0.1 V drop across R12 is balanced by a 0.1 V drop across R1. Thus, 2.5 μA flows into the collector of Q4.

The action of the DC feedback loop causes the Q1, Q2 amplifier output (node 7) to drop toward ground until the base emitter junction of Q4 is forward biased to give a collector current of 2.5 μA. Thus, the feedback path sinks the DC current from R1.

This bias condition is maintained by the feedback loop. Thus, Q4 and Q5 split the 52.5 μA current in R5 in a 1:20 ratio for no current input from the photodiode. Looking into the input, the effective feedback resistance is 20 times R5, or 20K.

The action of the averaging capacitor in the feedback loop is similar to the DC feedback action. As the photodiode current increases (Manchester square wave as shown in Figure 10), the voltage across the AGC capacitor decreases by the average value of the node 7 waveform, which is one-half the peak value of the node 7 voltage. Because node 6 drops toward ground, Q4 forward bias will increase because its base voltage is constant, and a larger percentage of the current in the feedback resistor R5 will now flow in Q4. Thus, the effective feedback resistance seen by the input has decreased. The transresistance of the pre-amp is reduced. The variable transresistance is equivalent to changing the "gain" of the pre-amp, and thus the nomenclature AGC loop.

Since the AGC voltage (voltage change across the AGC capacitor) is equal to one-half the peak output voltage swing, the transresistance will go from 1/20 to 1 for a peak output swing of 0 to 0.5 V. At 0.5 V, the feedback resistor R5 is 1 K. Thus, a photodiode current of 0.5 mA will produce full AGC action.

The current ratio between Q4 and Q5 is the transresistance factor M and is:

$$M = \frac{I_{Q4}}{I_{Q4} + I_{Q5}} = \frac{e^{[q/kT(V_{BEQ4} - V_{BEQ5})]}}{e^{[q/kT(V_{BEQ4} - V_{BEQ5})]} + 1}$$

The peak output swing is e_o, the feedback resistance is R_f, and the photodiode signal current (not including dark leakage current) is I_s.

$$e_o = I_s R_f = I_s \frac{1\,K}{M} \text{ and } I_s = e_o \frac{M}{1\,K}$$

The difference in base emitter voltages of Q4 and Q5 for no signal input is $V_{BEQ4} - V_{BEQ5} = -77$ mV.

Therefore, an approximate expression for the signal current as a function of e_o is:

$$I_s = e_o \frac{e^{[q/kT(e_o/2 - 77)]}}{e^{[q/kT(e_o/2 - 77)]} + 1}$$

where e_o is in mV and I_s is in μA.

A plot of this AGC characteristic is given in Figure 11. M is essentially equal to one and therefore $R_f = 20$ K at $I_s = 400$ μA. For $I_s > 400$ μA, $R_f = 1$ K; therefore e_o increases linearly up to the maximum 1 V. This maximum is controlled by Q116. The nominal voltage at node 9 is +1.1 V. With a maximum 1 V swing, this reduces to 0.1 V. The Schottky diode on Q116 prevents saturation and the resulting signal distortion for large swings. Input signal current in excess of 1.0 mA cannot be absorbed by the feedback loop. Therefore, Q1 is provided with a Schottky diode to shunt any excess current over 1 mA. However, once excess current flows in Q1, the bias conditions are upset and the signal will be distorted. This condition can also exist when the "gain" is maximum and a large start-up signal comes in before the gain can be reduced.

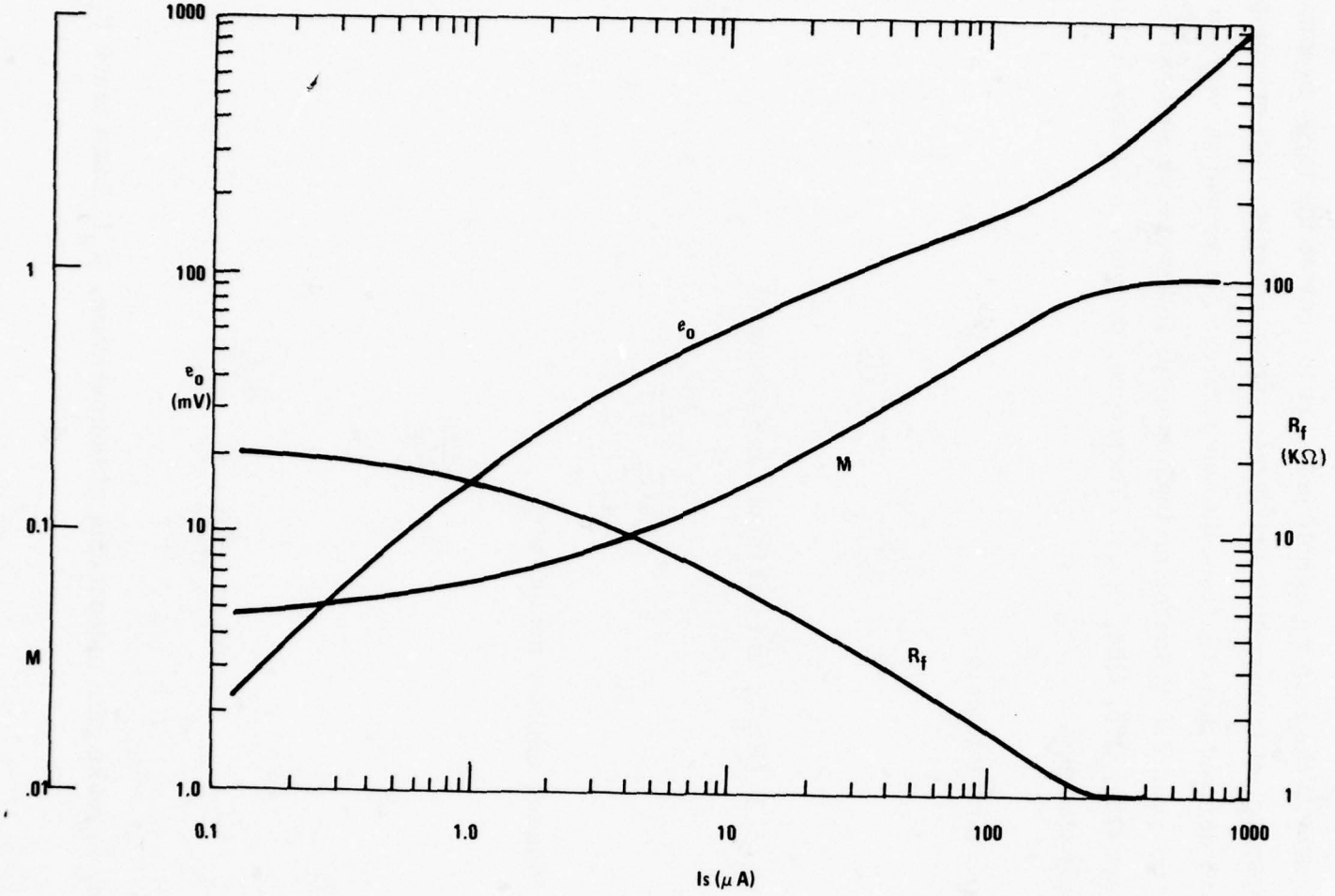


Figure 11. AGC Characteristic

The "gain" around the loop $A\beta$ is held constant to provide the large dynamic range independent of temperature and power supply changes. All pre-amp currents are derived directly from the temperature compensated, voltage regulated, constant 3.9 V source or from emitter followers whose base is tied to it (see Q20, Q65, Q66, etc.). Therefore, the gain is independent of power supply changes.

The gain around the loop is:

$$A\beta = \frac{R_T R_2}{R_f r_e} \quad \frac{1}{j\omega R_T C_T}$$

when $\omega R_T C_T > 1$ ($R_T C_T$ is total input time constant)

$$A\beta = \frac{1}{j\omega C_T} \quad \frac{R_2}{R_f r_e}$$

and r_e is dynamic emitter resistance

$$r_e = \frac{kT}{qI_E}$$

so

$$A\beta = \frac{1}{j\omega C_T} \quad \frac{q}{k} \quad \frac{R_2 I_E}{R_f T}$$

Therefore, to make gain independent of temperature, $R_2 I_E$ must track $R_f T$.

R_f is held constant by the AGC loop. The Q118 current source is held constant by the band gap regulator. The 1.7 V regulator output varies with temperature so that Q4 tracks the base currents Q1, Q11, and R1 changes. The feedback loop holds the collector current of Q4 constant at 2.5 μA. D2 tracks Q7 and the R5/R6 ratio is constant. The result of these effects is that the no signal transresistance factor is held to 1/20 independent of temperature. The feedback resistance R_f would vary as R5, but the current source Q116 tracks R2 in such a manner that R_f is constant over temperature.

Therefore, to hold Aβ constant, $R_L I_E$ must track T. T varies as +0.336 percent/° C and R_L (low ρ resistivity[3]) varies +0.12 percent/° C; therefore I_E must vary as +0.216 percent/° C. By giving the 1.7 V regulator a -2.15 mV/° C temperature coefficient and making I_E = 175 μA, with the R3, R17, D6 compensation network, I_E varies as +0.216 percent/° C. Therefore, Aβ is constant over voltage and temperature.

A noise analysis has been presented elsewhere[4], so only the results will be given here. Because of the presence of f^2 noise, the FORIC must have at least two poles in the high frequency cutoff characteristic so that the total noise will be bounded. The low frequency pole is at f_o and is:

$$f_o = \frac{1}{2\pi R_f C_f} = 13.5 \text{ MHz}$$

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[3] See Appendix A for details of the advanced bipolar process.

[4] J. R. Biard, "Optoelectronic Aspects of Avionics Systems," Final Report AFAL-TR-73-164.

the second pole is in the post-amp and is:

$$f_2 = 1.85\, f_o = 25 \text{ MHz}$$

The effective feedback resistance R_f varies from 20 K to 1 K over the dynamic range; f_o changes from 13.5 MHz at minimum signal to 24 MHz at maximum signal.

The emitter coupled input transistors Q1 and Q2 have a size ratio of 1:10. Q2 has 10 times the area of Q1 and carries 10 times the current. Thus, the V_{BE} of Q1 and Q2 are equal and give drift cancellation. However, r_e on Q2 is 1/10 of r_e on Q1 so that the gain and noise of the input stage is controlled by Q1.

Resistor R2 is a special "zero effective capacitance" resistor to minimize the input noise. The network consisting of Q20, Q21, D4, R22, and R26 supplies a signal on node 72 which is equal to the signal on node 3. The other ends of R2 and R_{epi} (the region surrounding R2) are tied to 3.9 V. Thus, there is no voltage difference across any element of the distributed capacitance between R2 and R_{epi}. See "Model for Special Resistor R2" in Section 5 for a complete description of R2.

Assuming a total input capacitance of 6.5 pF including the external photodiode plus stray capacitance, equivalent input resistance at minimum signal is 6.8 K. "White" noise at zero photodiode current is:

$$\frac{i_n^2}{\Delta f_W} = 2qI_{BQ1} + \frac{4kT}{R_f} + \frac{4kT}{R_1} + 2q\,(2.5\ \mu A)$$

The f^2 noise is:

$$\frac{i_n^2}{\Delta f_{f^2}} = \omega^2 C_T^2 \, 2.2k \, T \, r_e \text{ where } r_e = \frac{kT}{q \, I_E}$$

Minimizing the noise terms containing emitter current in Q1 yields an optimal value

$$I_{E_{OPT}} = 175 \ \mu A$$

The total rms equivalent noise is

$$i_{n_{TOTAL}} = 7.54 \text{ nA for minimum input signal}$$

When R_f = 20 K and $i_{n_{TOTAL}}$ = 7.54 mA, the response of the circuit is basically a two pole network with $a_1 = f_o/f_2 = 0.54$.

For 10 MHz square wave,

$$\frac{e_s}{I_s R_f} = 1/2 \frac{[1 - \delta(T/2)]}{[1 + \delta(T/2)]} = 0.47$$

Thus, to achieve 10^{-8} BER, I_s must be (1/0.47) (5.62) = 12 times larger than the rms $i_{n_{TOTAL}}$ for a single comparator on the output.

$$I_{s_{min}} = (12) \, (7.54 \text{ nA}) = 90.5 \text{ nA}$$

at 125 nA input, there is 125/90.5 = 1.38 or 2.8 dB electrical excess S/N at 25° C.

The change in noise as temperature increases from 25° C to 125° C is:

- White noise decreases 16.4 percent.
- The f^2 noise increases by a factor of 1.78.
- $i_{n_{TOTAL}}$ increases from 7.54 nA to 7.57 nA, a 0.3 percent change.

The pulse jitter due to noise is developed in detail in Appendix B. The result of that analysis is that the rms jitter of the received signal is 3 ns for BER = 10^{-8}.

POST-AMPLIFIERS

Both post-amplifiers are differential stages with temperature compensated gains of 14 (see Figure 12). Both have diodes in their collector circuits (D7, D8, D34, D35) to limit the output swings to one diode drop. Because of the low supply voltage (3.9 V - V_{BE}) applied to the load, a large signal swing can saturate the differential amplifier and distort the signal. The collector diodes prevent this.

AC coupling between the two post-amps is accomplished with an external coupling capacitor. A unique feature of this coupling is the manner in which the differential amplifier reference is derived. One emitter follower (Q30) output DC couples through R31 and R46 into both inputs and biases them at the same level. The AC coupling feeds one half of the differential amplifier and effectively swings the total signal.

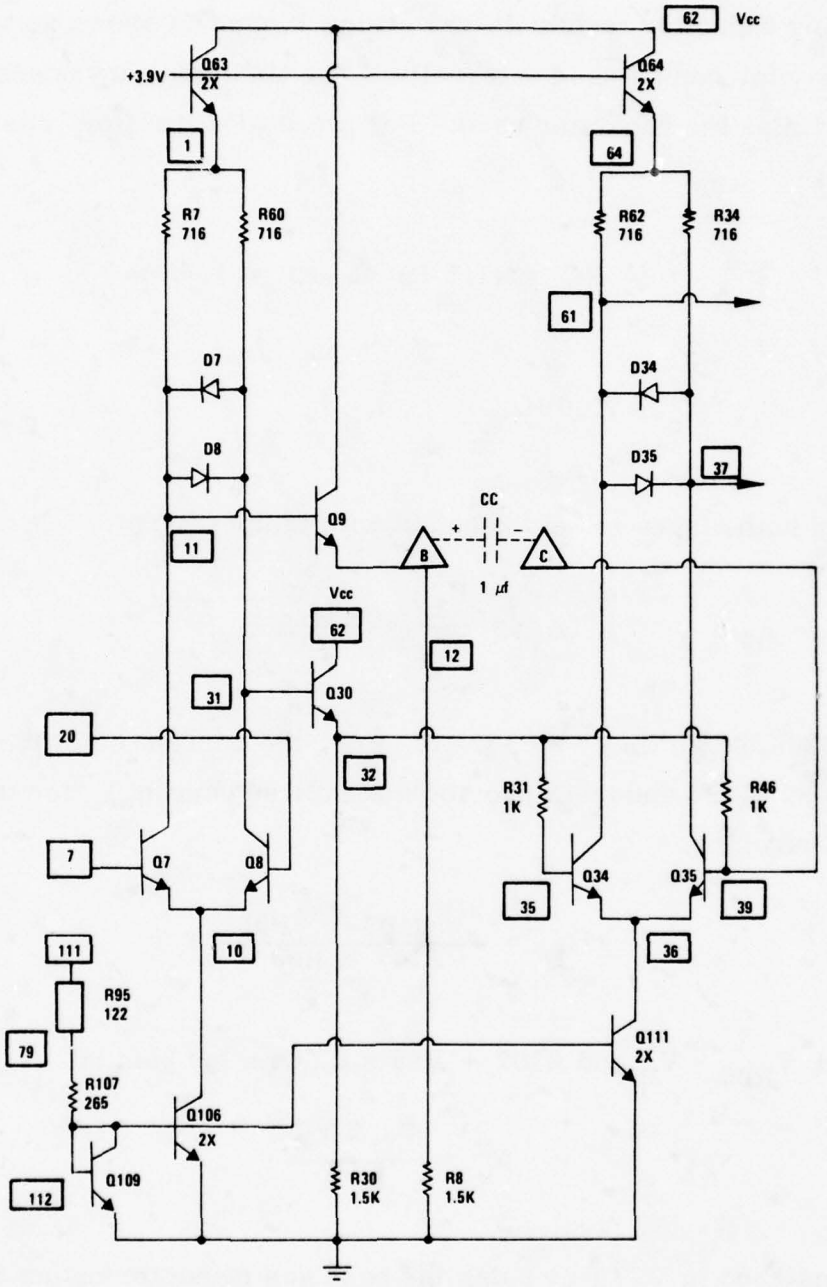

Figure 12. Schematic of First and Second Post-Amp Stages

The coupling capacitor terminals are always biased as shown so that a polarized capacitor can be used externally. The time constant is essentially R = 1.5 K times the capacitor used. For a 1.0 μF capacitor, one time constant is

$$\tau = RC = (1.5\ K)\ (1\ \mu F) = 1.5\ ms$$

so

$$f_c = 100\ Hz$$

The gain of both stages is held constant with temperature.

$$A_v = \frac{R_L}{2r_e} = \frac{R_L\, q\, I_E}{2kT}$$

Because Q106 is two times the size of Q109, the current in Q106 is twice that in Q109. Q106 and Q111 provide the emitter current I_E for the two stages. Therefore,

$$I_E = \frac{2(V_{R107} + V_{R95})}{R107 + R95}$$

If $V_{R107} + V_{R95} = V_R$ and R107 + R95 = R, then the gain is

$$A_v = \frac{R_L\, q\, V_R}{kTR}$$

R_L/R is matched to V_R/T by using the band gap regulator output and the ratio of R95 to R107 with their different temperature coefficients.

OUTPUT STAGES

There are two stages in the output circuit of the FORIC as shown in Figure 13. The first is a level translator, the second a TTL buffer.

The output of the second post-amp stage is a differential signal referenced to 3.9 V. This signal must be translated to a signal referenced to ground so that the TTL buffer can "square it up" for presentation to the output pin. Translation is accomplished by a cross coupled pair of current mirrors. Transistors Q31, Q32 with R64 forms one current mirror, and its output drives the input of Q43, Q44 with R63 current mirror. The current through R64 or R63 is split between the two current mirrors in such a manner that the total current is constant. The operation is similar to a flip-flop.

Schottky diodes D32 and D44 clamp the collectors of Q32 and Q44 so that they do not saturate. D32 and D44 clamp without stealing any current from either base. The Schottky diodes get their current from R65, and their input voltage is clamped to the same level as the bases of Q32 and Q44 by diode D65.

The two current mirrors not only translate the second post-amp output voltage swing down to ground, they also convert the signal from a voltage to a current. Therefore, the current in Q32 is mirrored in Q33, and Q44 current is mirrored in Q45. Resistors R32 and R33 change the signal back to a voltage swing that drives the TTL buffer. Schottky diodes D32, D33, D44, and D45 prevent transistor saturation without stealing any base current. Diode D9 is in series with R33 to maintain equal voltage swings across R32 and R33; it clamps the bottom end of R33 at two V_{BE}'s above ground the

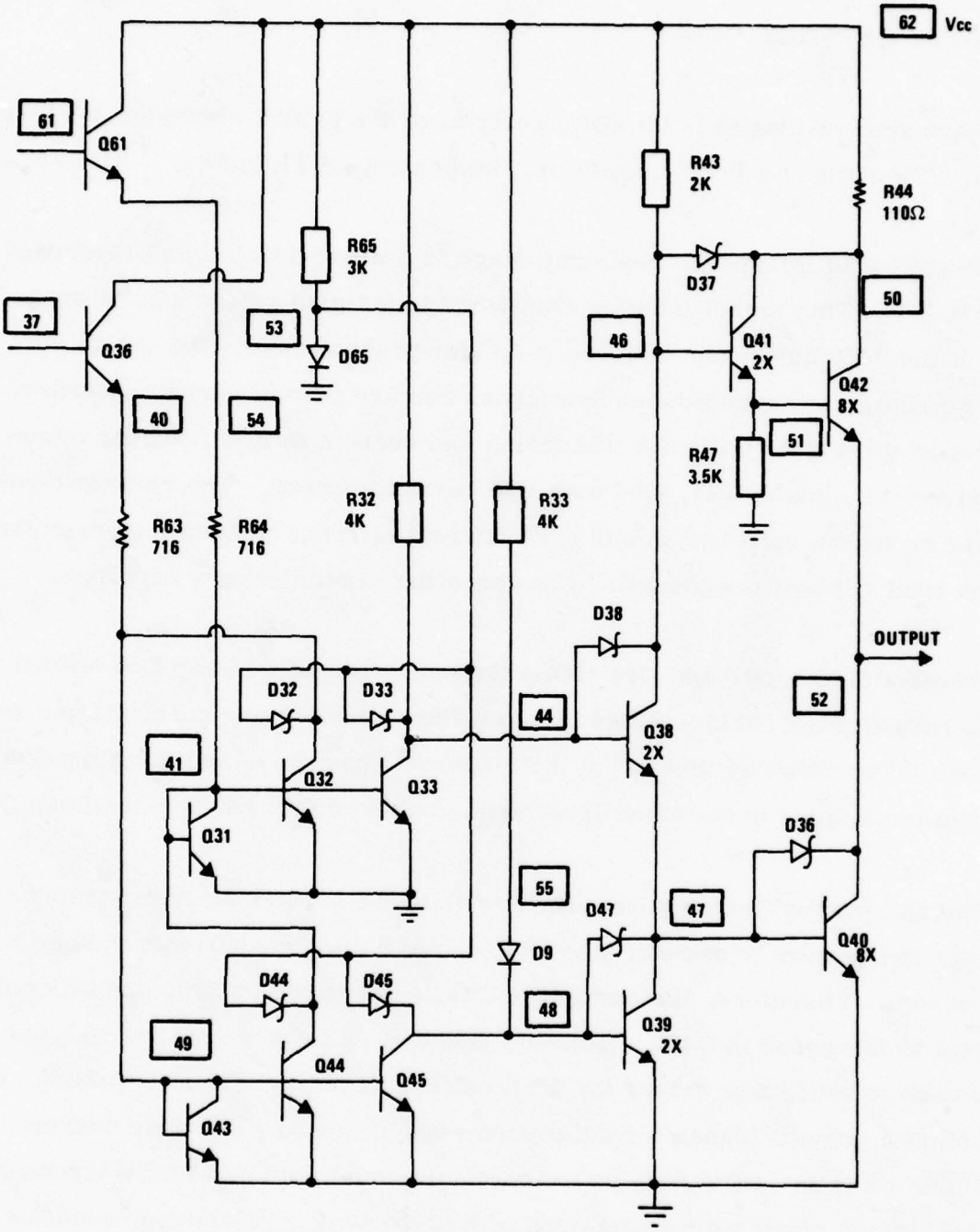

Figure 13. Schematic of Output Stages

same as Q38 and Q40 clamp the bottom of R32. The currents in these two clamped paths are not identical but are very close allowing nodes 44 and 55 track over temperature.

The input to the TTL gate is a linear voltage swing. All the transistors in the TTL output stage are Schottky clamped and divert current from their bases into the Schottky diodes. The values and connections are identical to standard Schottky TTL gate outputs, except the Schottky diode D36 is sized to give the standard 5400 TTL output "0" level of 0.4 V instead of the Schottky TTL 0.5 V level.

The gain of the output stages varies as one-half the transistor's beta or $\beta/2$. Therefore, it is not constant with temperature.

The output of the second differential stage is approximately a 0.4 V swing with the minimum current (125 nA) signal into the pre-amp. The worst case β is at low temperatures and can be as low as 40. Given the fact that the minimum input signal does not cause the post-amp stages to limit (collectors clamped by diodes across them), the gain of the output stage is still sufficient to guarantee full TTL output swing with much less than the minimum signal. As a matter of fact, the output follows the noise on the input when no signal is present. The output swings full amplitude with noise so that there is never a problem of leaving the output "half-on" and causing input problems for a TTL gate driven by the FORIC.

BAND GAP REGULATOR

The detailed design approach to synthesize a band gap regulator is well documented.[5,6] Essentially, the most stable and predictable property of a silicon transistor, the base emitter voltage (V_{BE}), is used as a reference to generate a voltage with a given temperature coefficient (TC) which becomes the output of the regulator.

Referring to Figure 14, transistors Q104 and Q108 are run at different emitter current densities (J). The emitter current in Q104 is the same as in Q108, but the emitter size of Q104 is 10 times Q108, so $J_{Q108} = 10\ J_{Q104}$. This difference results in a V_{BE} difference of

$$\Delta V_{BE} = \frac{nkT}{q}\ \ell n\ \frac{J_{Q104}}{J_{Q108}} = \frac{nkT}{q}\ \ell n\ 10$$

where

T = ° K

k = Boltzman's constant

q = electronic charge

n = process constant

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[5] Robert Dobkin, "1.2-Volt Reference," National Semiconductor Application Note AN-56, National Semiconductor Corp., Santa Clara, 1971.

[6] Alan B. Grebene, Analog Integrated Circuit Design, New York: Van Nostrand Reinhold, 1972.

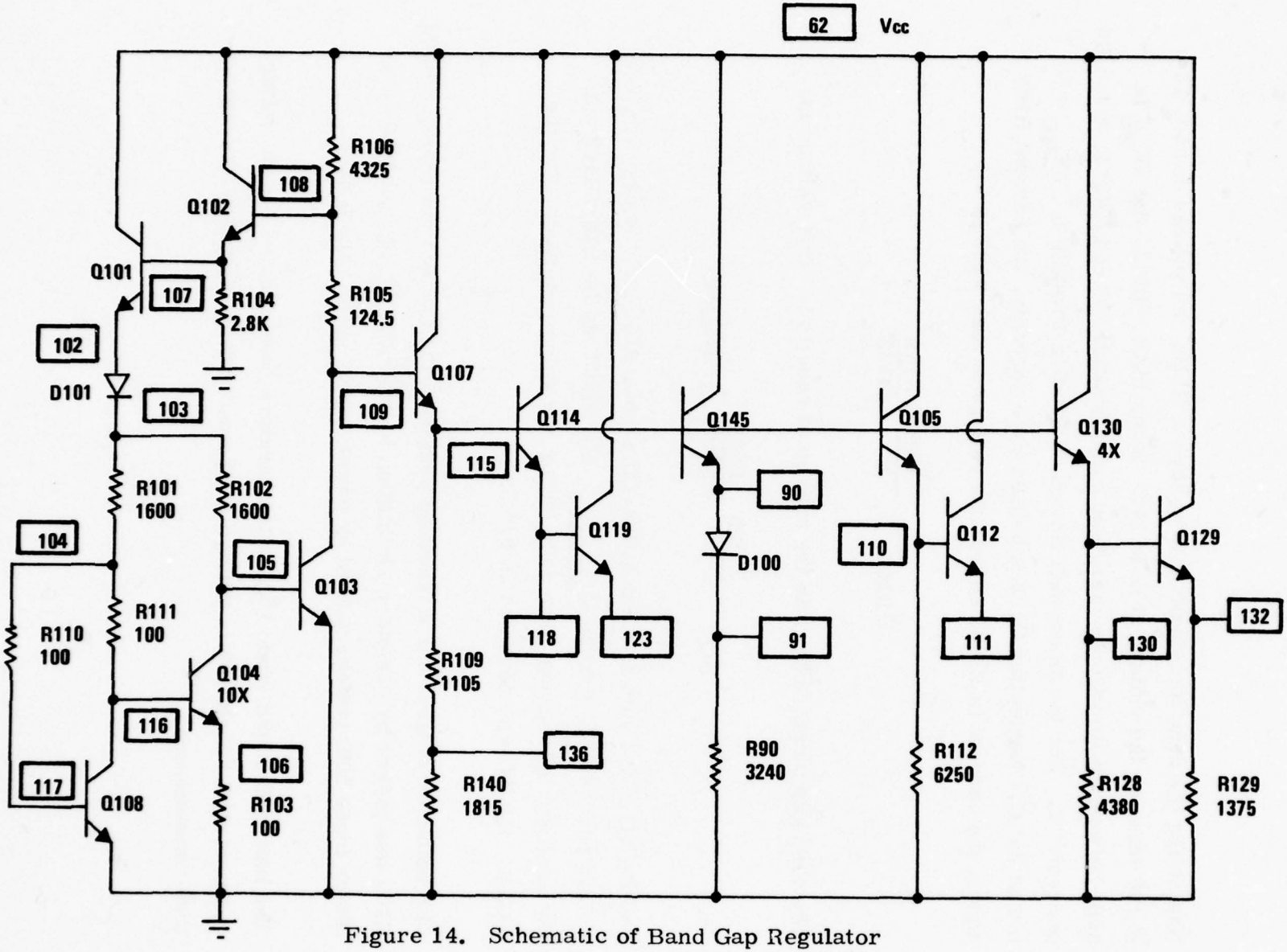


Figure 14. Schematic of Band Gap Regulator

Neglecting the drop (nominally 1 mV) across R110, the voltage at node 104 is the same as the voltage at node 117. Since R103 = R111, the ΔV_{BE} is split between these two resistors and has a positive TC of $1/273^\circ$ K $\approx +0.36$ percent/° C. For the Honeywell Advanced Bipolar Process I,[3] $\Delta V_{BE} \approx 59.7$ mV at 25° C. Neglecting Q103 and Q104 base currents, the current R102 equals the current in R103, so that the voltage across R102 is

$$V_{R102} = \frac{\Delta V_{BE}}{2} \frac{R102}{R103}$$

The band gap output voltage is the voltage at node 103. This voltage is

$$V_{BG} = \frac{\Delta V_{BE}}{2} \frac{R102}{R103} + V_{BEQ103}$$

and its TC is the sum of the positive TC across R102 and the negative TC (-0.36 percent/° C) across $V_{BE\ Q103}$. By adjusting the R102/R103 ratio, the band gap voltage can have zero TC or any value required. For the FORIC, the TC was designed as 0/° C.

The collector of Q103 has a feedback path back to node 102 via resistor R105. R105 was picked by computer simulation to minimize changes in Q103 collector (node 109) voltage caused by power supply (Vcc) variations.

The band gap output (node 103) is temperature compensated but not voltage compensated. Node 109 is voltage compensated but only partially temperature compensated.

Various voltage levels with either zero TC, or one or two V_{BE} levels above this zero RC voltage were required. These voltage levels required voltage compensation. To accomplish this, the band gap output (node 103) was shifted up three V_{BE}'s--D101, Q101 and Q102--then back down with Q107 acting as the common drive point. The final temperature and voltage compensated outputs appear on nodes 123, 91, 111, and 132.

In selecting values of emitter currents for the transistors driven by Q107, the emitter current densities were chosen so the total V_{BE} temperature dependence would match with that of devices Q101 and D101. Resistor R104 was chosen to match the emitter current density of Q102 to Q107 so their V_{BE}'s would track with temperature.

3.9 V REGULATOR

To eliminate the effects of a 20 percent variation in Vcc (i.e., 4.5 V $\leq$ Vcc $\leq$ 5.5 V) the circuitry in the pre-amp and the post-amp stages are powered from a 3.9 V regulated supply. To minimize the loading of this supply and thereby simplify its design, the 3.9 V is used in most cases to provide only base current to emitter followers whose collectors are then tied directly to Vcc. Transistors Q63, Q64, Q65, and Q66 are examples of this "load minimizing" (see Figure 9, page 2). The emitter followers lower the regulated voltage by one V_{BE}.

The final regulated voltage is equal to 3.9 V - V_{BE}, and it varies with temperature as a V_{BE}. The total current supplied by the 3.9 V regulator under nominal conditions is 1.5 mA. The circuitry for the 3.9 V regulator is shown in Figure 15.

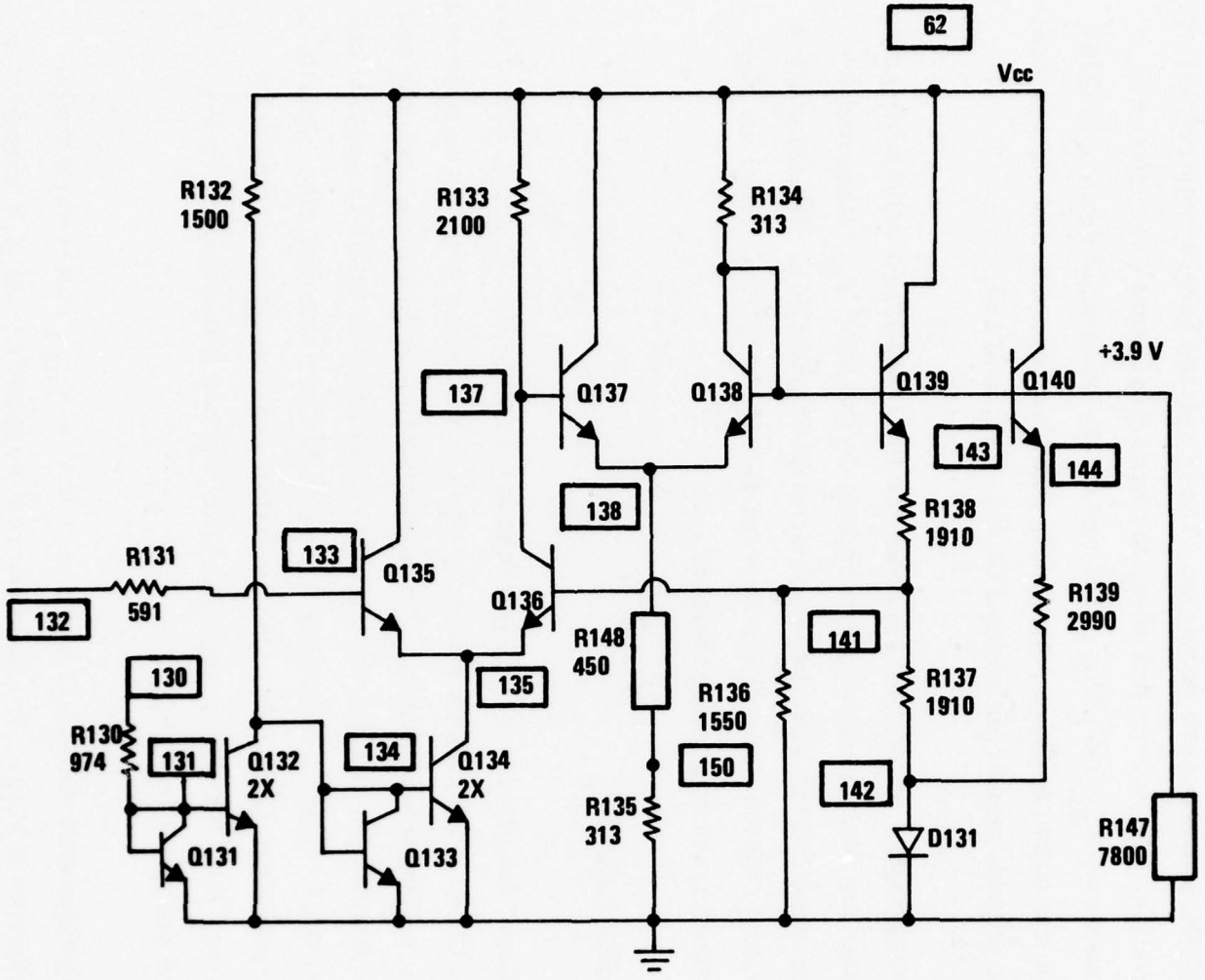


Figure 15. Schematic of 3.9 V Regulator

The 3.9 regulator input nodes 130 and 132 come from the band gap regulator. Node 132 is the zero temperature coefficient, voltage compensated band gap voltage while node 130 is one V_{BE} above this, and it varies with temperature as a V_{BE}. Node 131 also has a V_{BE} voltage temperature coefficient. The total current through resistor R130 varies according to the temperature coefficient for low ρ-resistors or 0.12 percent/° C. Q132 is a 2X device. Therefore, its emitter current is twice the current in R130 and has this resistor's temperature coefficient. Therefore, the voltage across R132 (for nominal Vcc) remains constant. Since node 134 is clamped at a V_{BE} by Q133, any excess current through R132 caused by an increase in Vcc is absorbed by Q133. Transistor Q134 is a 2X device and its emitter current will be twice the current in Q133. Thus, the current in Q134 changes only with Vcc changes, not with temperature.

The "reference node" for the 3.9 V regulator is node 137. The voltage on node 137 is simply "mirrored" over to the 3.9 V output by transistors Q137 and Q138. Both of these devices have approximately the same V_{BE} at nominal supply voltage. The differential amplifier formed by Q135 and Q136 tries to maintain node 141 at the same voltage as node 133 (i.e., the zero temperature coefficient band gap voltage). The output voltage of this amplifier appears at node 137 and is compensated for variations in supply voltage as follows. As Vcc increases, the current in R132 increases. Since the collector current in Q132 is fixed by the current in R130 which is supply independent, the excess current in R132 is absorbed by Q133. The collector current of Q134 then increases and so does the voltage drop across R133. This acts to bring node 137 back down.

Transistor Q137 functions as an emitter follower off of node 137. This minimizes the loading on this node and prevents disruption of the regulator. It also shifts the node 137 voltage down by one V_{BE}. The regulated voltage appears at node 138 reduced by one V_{BE}. Transistor Q138 is connected as a diode to shift the regulated node 138 voltage back up to the desired regulated output voltage. This shift down then back up approach is used to obtain the highest regulated voltage possible with a low Vcc voltage of 4.5 V. Other approaches suffer a V_{BE} drop, which puts the regulated voltage at less than 3.9 V. Therefore, node 137 is regulated at 3.9 V, then is shifted down by a V_{BE} (Q137), and then back up by a V_{BE} (Q138). Resistors R135 and R148 serve as a resistive current source for Q137 and Q138 and are chosen for a nominal current of 4.0 mA.

Resistors R137 and R138 are the principal feedback resistors that temperature compensate the 3.9 V output. Node 141 is held at the zero temperature coefficient band gap voltage on node 132 by the Q135-Q136 differential amplifier. Transistor Q139 decouples the current flowing in R137 and R138 from the 3.9 V supply, minimizing the total current loading on the 3.9 V output. If the base of Q136 and R136 were disconnected from node 141, the voltage that would appear at the intersection of R137 and R138 would be 3.9 V/2. However, node 141 is maintained at the band gap voltage (approximately 1.2 V). Adding resistor R136 pulls more current through R138, dropping the extra voltage to maintain the 3.9 V on the base of Q139. Adding R136 pulls more current through Q139 also, and thus is no longer equal to the current in D131. Adding transistor Q140 and resistor R139 increases the current in D131 to the same value as in Q139. Q139 and D131 now track each other over the temperature range and compensate the 3.9 V output.

After computer simulation of the complete receiver circuit, the load current pulled from the 3.9 V regulator was found to have a positive temperature coefficient which affected the 3.9 V with temperature. Resistor R147 was added and the ratio of R148 and R135 was determined to correct the load current variation and thus stabilize the output voltage at 3.9 V.

1.7 V REGULATOR

The 1.7 V regulator derives its reference voltage from the band gap regulator. Resistors R109 and R140 (see Figure 14) form a resistive divider which takes the band gap node 115 voltage and divides such that

$$V_{\text{Node 136}} = V_{\text{Node 115}} \quad \frac{\text{R140}}{\text{R109+R140}}$$

Under nominal conditions the voltage at node 115 is 2.747 V. Therefore, the voltage at node 136 is 1.707 V.

The 1.7 V regulator is a voltage shunt feedback amplifier (see Figure 16). To improve regulation and maintain a low noise output, the 3.9 V regulator has been used as the reference power source. The collector current of Q141 and the current in R143 power the 1.7 V regulator. The collector current of Q143 is the current in R143 less the base current for Q146. The feedback path that regulates the 1.7 V is from node 139 to node 149 via Q146. For example, a rise in the 3.9 V supply will result in a rise in voltage at node 139. This means that node 149 will also rise in voltage because of Q146 V_{BE}. The increased voltage at node 149 will cause an increased collector current in Q143 and a larger drop across R143. This will bring

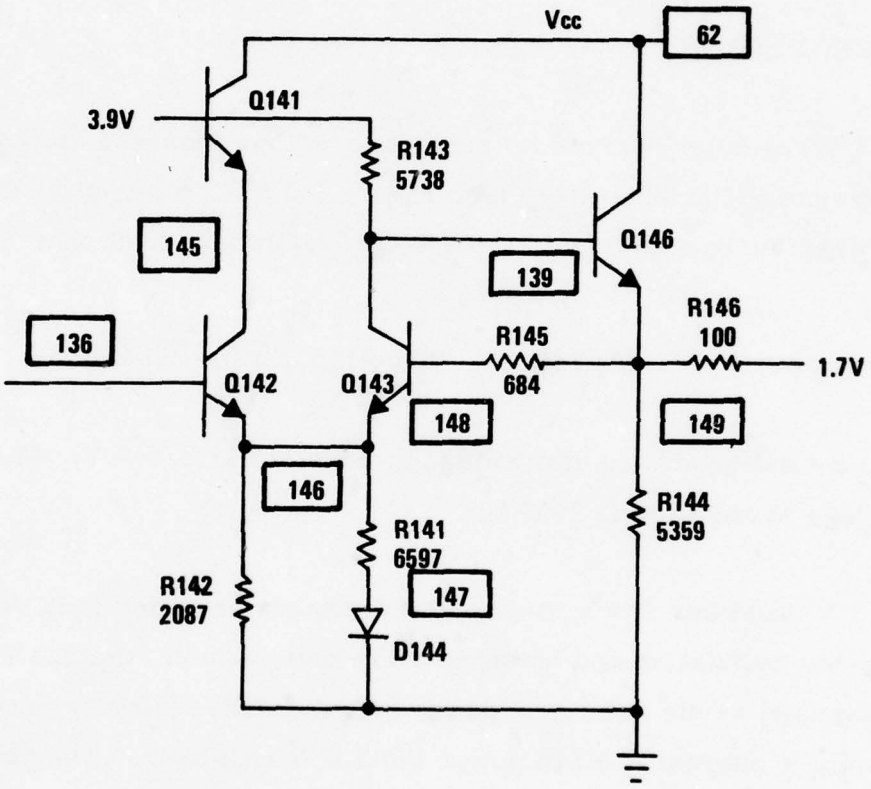


Figure 16. Schematic of 1.7 V Regulator

node 137 back down and reestablish node 149 at 1.70 V. Only a few microamps base current (see Figure 9, page 1) are pulled from the 1.7 V regulator; the drop across R146 can be neglected. The base current drawn by Q143 flows across R145 and accounts for the slight difference in voltage between nodes 136 and 149. The 1.7 V regulator output voltage was designed to have a -2.15 mV/° C temperature coefficient. Resistors R142 and R141 along with D144 establish this TC.

SECTION V

DEVICE PARAMETERS

The initial synthesis of a circuit can be realized using estimated values for device parameters. However, before circuit simulation can be finalized and the layout completed, the device parameters must be derived for the specific size devices to be used.

TRANSISTOR PARAMETERS

There are 79 transistors and 14 diodes (transistors with their base shorted to collector to form a diode) used in the FORIC. However, there are only 13 different sizes of three transistor types. Two of the types can be distinguished by the shape of their emitter (square or rectangular). The third type is a Schottky diode clamped rectangular emitter transistor. Therefore, there are actually only two basis transistor styles used in the FORIC design.

Figure 17 shows the square emitter style transistor. This style is also characterized by the placement of the base between the emitter and collector, termed EBC structure. This square emitter EBC style transistor provides:

- The smallest ratio of emitter periphery to emitter area to insure the best V_{BE} matching.
- A wide base relative to emitter width for low base resistance and effective use of all four emitter edges.

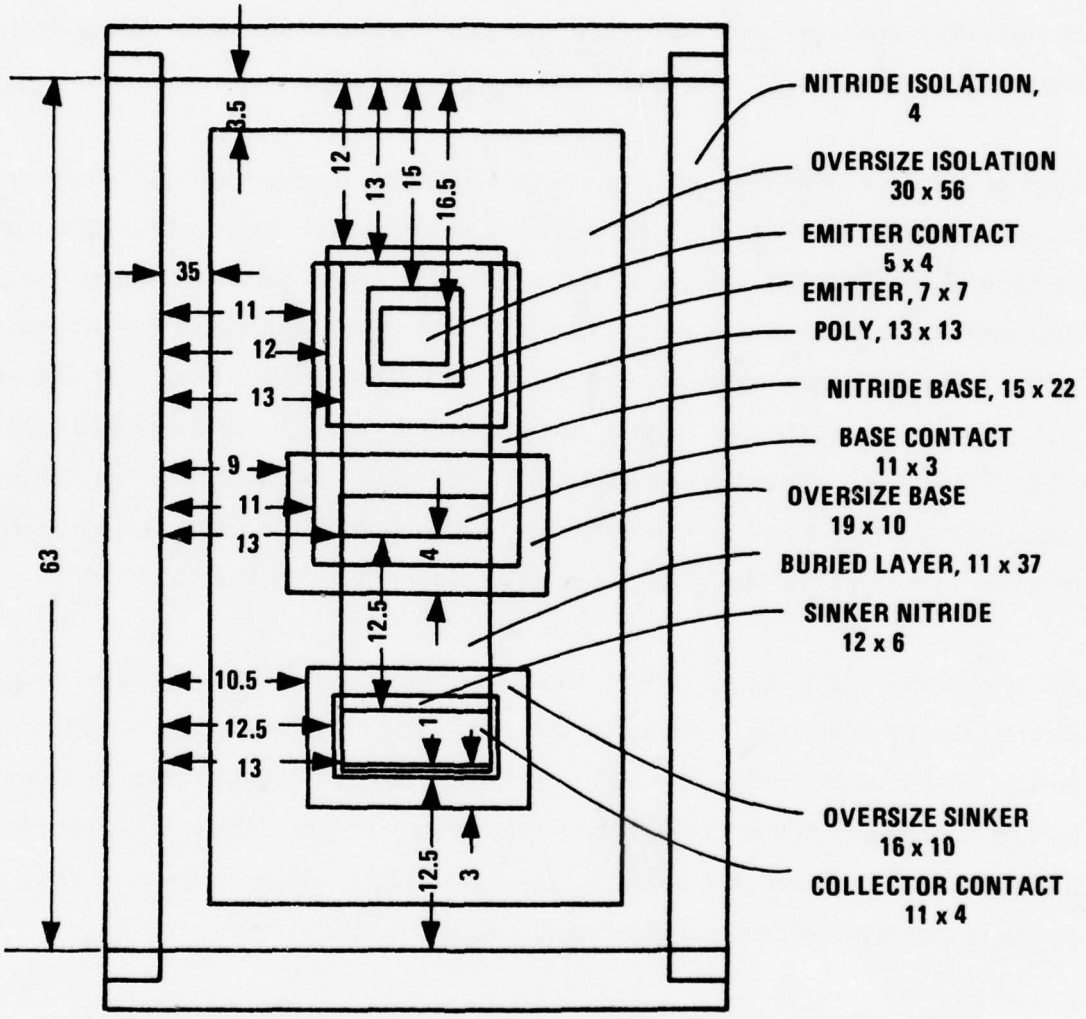


Figure 17. Square Emitter EBC Transistor

This style transistor is used in the regulator portion of the FORIC where V_{BE} matching and emitter efficiency are critical characteristics. The square emitter EBC structure has more base-collector capacitance than the rectangular emitter BEC structure; for the regulator circuits, however, this characteristic is less important than V_{BE} matching.

Figure 18 shows the rectangular emitter BEC style transistor. This style transistor with and without a Schottky diode clamp is used in the signal path portion of the FORIC because of the minimized base-collector capacitance that provides maximum speed. The BEC structure permits easy placement of the Schottky diode contact over the base-collector junction. For the specially clamped transistors in the cross-coupled comparitor stage (Q32, Q33, Q44, Q45), the rectangular emitter BEC structure is used, but the Schottky diode contact is placed on the collector end opposite the base end in such a manner that the Schottky diode node is not connected to the base.

All transistor sizes were chosen to insure that they operate on the linear side of the f_T peak (i.e., less than the peak shown in Appendix A, Figure A-4). The emitter current density of the transistor used to plot that curve is 0.026 mA/μ^2. When the emitter area of any of the FORIC transistors is multiplied by this current density, the resulting number is greater than or equal to the typical current flowing through the transistor.

Figure 19 shows a cross section view of a transistor with various equations for calculating the parameters of a transistor. Table 6 summarizes all the data generated for the FORIC transistors and diodes by using Figure 19. The headings in Table 6 list the 13 different transistor/diode sizes by number (see Figure 9 to identify the Q number position in the circuit). Table 7

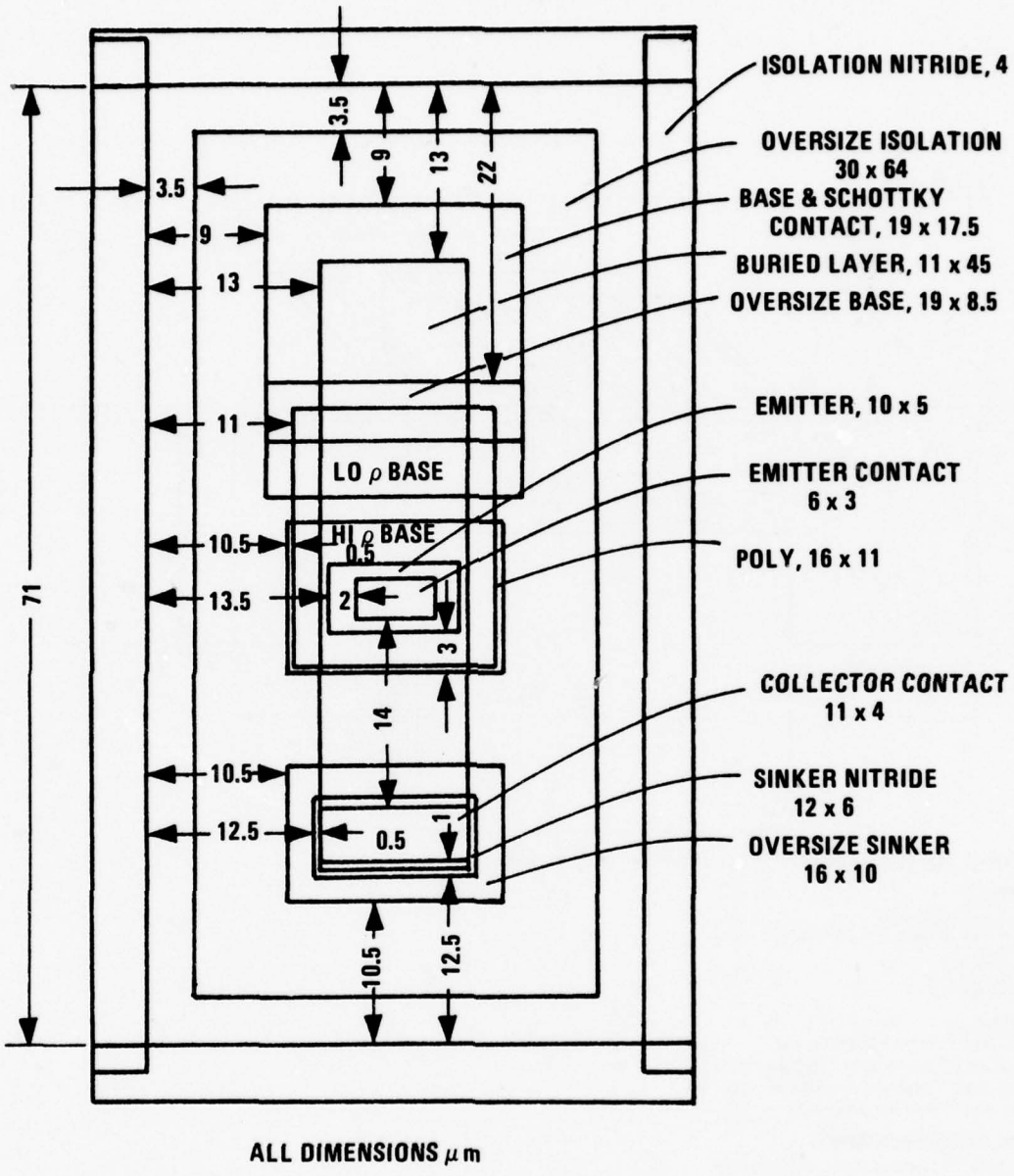
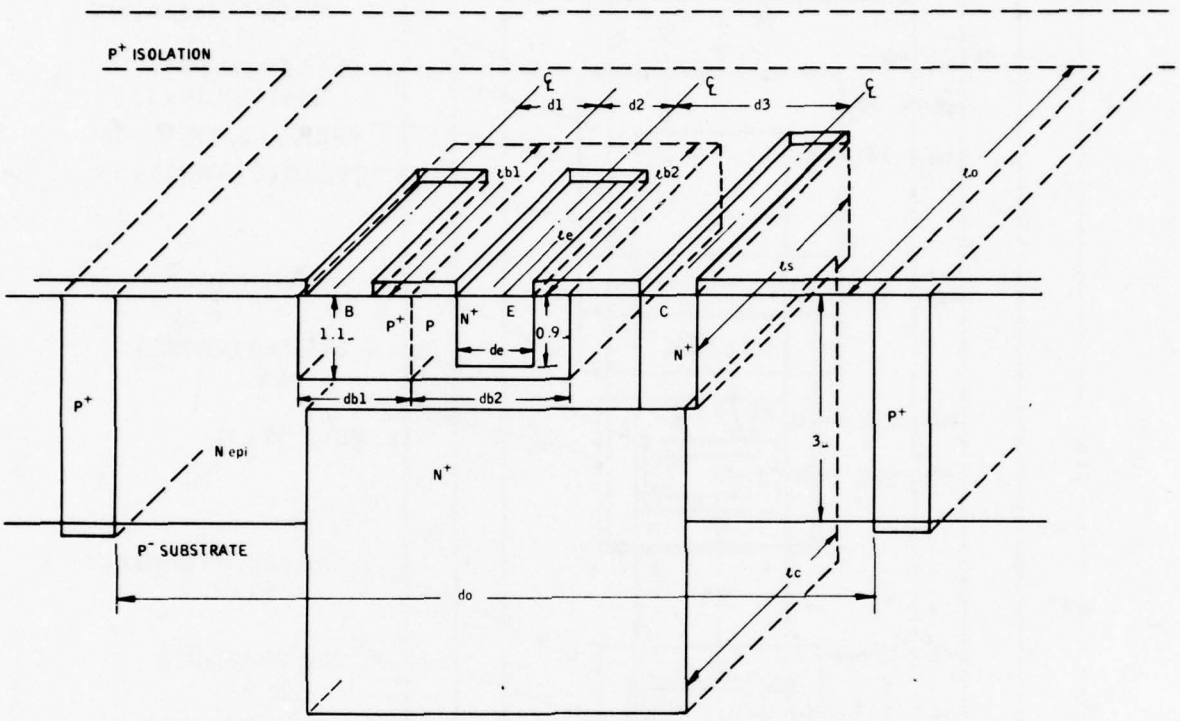


Figure 18. Rectangular Emitter BEC Transistor with Schottky Diode Clamp



APPROXIMATE SCALING RELATIONSHIPS [ALL DIMENSIONS ARE IN MICRONS (μ)]

RESISTANCES:

RE = 0.7/N + 480/(ℓe*de)
N=1 FOR 1X SIZE, N=2 FOR 2X SIZE, ETC.
RS = 75/ℓs Ω
RC = 8.6*d3/ℓc Ω
RB1 = 266*d1/ℓb1 Ω
RB2 = 240*d2/ℓb2 Ω

CAPACITANCES:

CBE = $2.8*10^{-3}$ [de*ℓe + 0.9*2(de+ℓe)] pF
CB1C = $4.8*10^{-4}$ [(db1*ℓb1) + 1.1*2(db1+ℓb1)] pF
CB2C = $4.8*10^{-4}$ [(db2*ℓb2) + 1.1*2(db2+ℓb2)] pF
CCS = $3.1*10^{-4}$ [(do*ℓo) + 3*2(do+ℓo)] pF

REVERSE SATURATION CURRENTS:

IES = $1.2*10^{-18}$ [(de*ℓe) + 0.018*2(de+ℓe)] AMPS
ICS = $2.4*10^{-19}$ [(de*ℓe) + 0.33[(db1*ℓb1) + (db2*ℓb2) - (de*ℓe)] + 0.37[2(db1+db2)+(ℓb1+ℓb2)]] AMPS

Figure 19. Cross-Sectional View of Transistor with Equations for Calculating Transistor Parameters

TABLE 6. CALCULATED TRANSISTOR MODEL PARAMETERS

Transistor Parameters	Q1	Q2	Q3	Q16	Q32	Q38	Q40	Q42	Q101	Q104	Q130	Q116	Q132	D2
Resistance														
Base R_B, Ω	191.5	18.76	162.5	87.8	162.5	113.5	36.6	30.9	175.9	24.3	57.1	191.5	103.8	9.38
Collector R_C, Ω	6.02	.916	6.19	3.78	6.02	3.96	1.38	1.38	9.98	1.76	3.9	6.02	6.56	.458
Emitter R_E, Ω	5.61	.516	5.61	2.81	5.61	3.13	1.35	1.35	5.80	.58	1.45	5.61	2.90	.281
Sinker R_S, Ω	3.36	.451	1.18	1.96	3.36	2.12	.71	.71	3.36	.583	1.22	3.36	2.12	.451
Current														
Emitter saturation I_{ES}, 10^{-16} A	1.18	11.80	.592	2.36	1.18	2.39	8.98	8.98	1.14	11.40	4.56	1.18	2.28	23.60
Collector saturation, I_{CS}, 10^{-16} A	.567	5.02	.377	1.08	.592	.984	3.19	3.19	.610	4.56	1.93	.567	1.05	10.04
Capacitance														
Base-emitter, C_{BE}, pF	.377	3.77	.377	.754	.377	.722	2.611	2.611	.361	3.610	1.444	.377	.722	7.540
Collector-base internal, C_{B1C}, pF	.135	1.167	.151	.264	.151	.218	.642	.642	.151	.976	.426	.135	.243	2.334
Collector-base external, C_{B2C}, pF	.132	1.093	.132	.239	.132	.219	.666	.666	.146	1.011	.435	.132	.242	2.186
Collector-substrate, C_{CS}, pF	.799	3.070	.553	.848	.835	.962	2.429	2.209	.607	2.765	1.326	.690	.847	4.638
Schottky Diodes														
Reverse saturation, Is, 10^{-12} A	1.02				2.10	3.35	5.69					2.10		
Resistance, R_{SH}, Ω	86.49				41.98	26.34	15.50					41.98		
Capacitance, C_{SH}, pF	.128				.264	.420	.714					.264		

$R_B = R_{B1} + R_{B2}$, nominal beta = 80, reverse beta = 5

TABLE 7. TRANSISTOR TYPES AND DUPLICATE TRANSISTORS

Q Numbers of the Thirteen Transistor Types	Rectangular Emitter BEC Structure		Square Emitter EBC Structure	Transistors/Diodes
	With Schottky	Without Schottky		
Q1	1X			---
Q2		10X		Q10, Q117
Q3		1X		Q4-Q9, Q11-Q15, Q19-Q21, Q30, Q31, Q34, Q36, Q43, Q61, Q65, Q66, Q90-Q93, Q109, Q115, D4-D9, D34, D35, D65
Q16		2X		Q17, Q18, Q63, Q64, Q106, Q111
Q32	1X			Q33, Q44, Q45
Q38	2X			Q39, Q41
Q40	8X			---
Q42		8X		---
Q104			10X	---
Q108			1X	Q101-Q103, Q105, Q107, Q112, Q114, Q119, Q129, Q131, Q133, Q135-Q143, Q145, Q146 D100, D101, D131, D141
Q116	1X			Q118
Q130			4X	---
Q132			2X	Q134
D2		20X		---

lists these same 13 Q numbers with their device sizes (2X, 8X, etc.) relative to the 1X transistors shown in Figures 17 and 18. Table 7 also lists the Q numbers of the duplicate transistors and diodes used in FORIC.

Figure 20 shows the model used for the transistors whose parameters are listed in Table 6.

SCHOTTKY DIODE PARAMETERS

The measured parameter values of a typical Schottky diode at 25 °C whose area is 144 μ^2 are as follows:

$$V_{forward} = 0.670 \text{ at } 1 \text{ mA},\ R_{SH} = 135\Omega,\ C_{SH} = 0.12 \text{ pF}$$

To determine the per unit area parameters, start with the contact potential, V_c:

$$V_c = \frac{n K T}{q}$$

where

n = 1.1
K = Boltzman's constant
T = °Kelvin
q = electronic charge.

Thus,

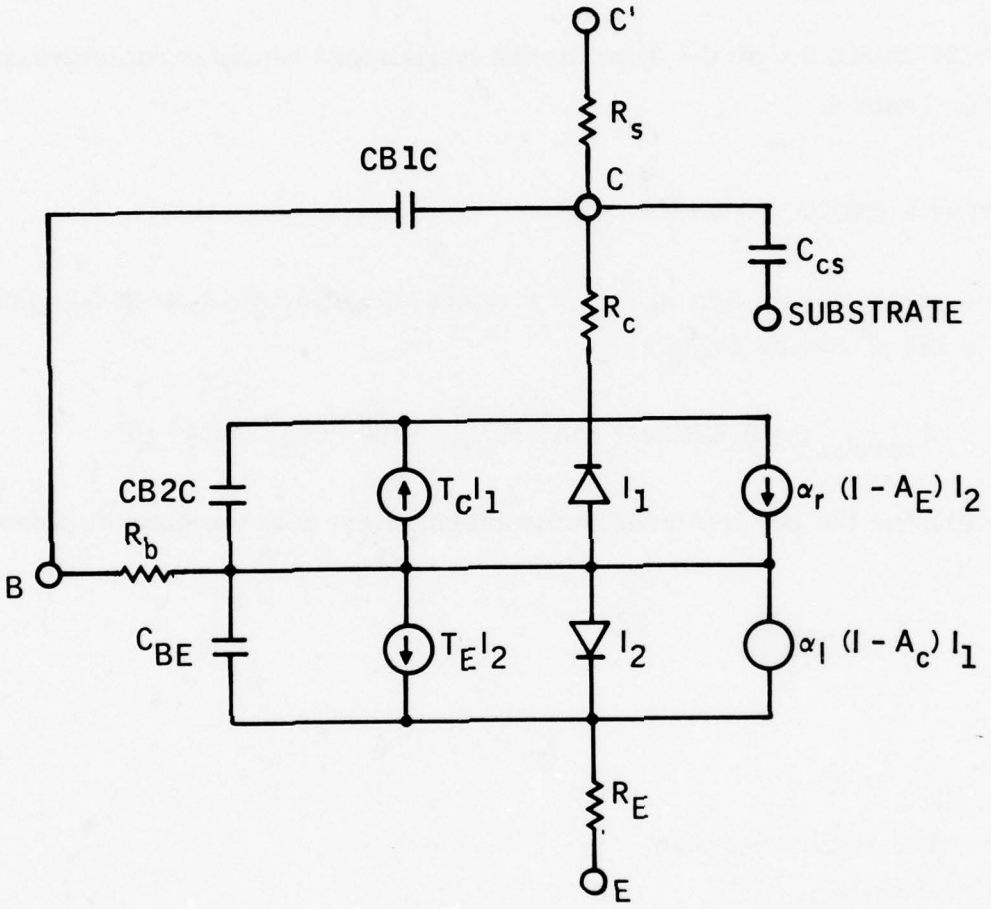


Figure 20. NPN Transistor Model

V_c = 0.020657 at -55°C

V_c = 0.028237 at +25°C

V_c = 0.040082 at +150°C

The reverse saturation current, I_s, is given as:

$$I_s = I_{SH}\, e^{-\frac{V_{SH}}{V_c}}$$

where I_{SH} and V_{SH} are the current and voltage of the Schottky diode without series resistance. Thus,

$$V_{SH} = 0.670 - (135)(0.001) = 0.535V$$

The capacitance is not a function of temperature, but the resistance has a +0.25%/° C temperature coefficient. Taking into account the 144 μ^2 area, the per unit parameters as a function of temperature is listed in Table 8.

TABLE 8. PER UNIT AREA SCHOTTKY PARAMETERS

Parameter	-55°C	+25°C	+125°C	Units
I_o	1.2×10^{-19}	4×10^{-14}	1.2×10^{-9}	A/μ^2
R_o	1.52×10^{4}	1.9×10^{4}	2.5×10^{4}	$\Omega\text{-}\mu^2$
C_o	---	8.3×10^{-4}	---	pF/μ^2

Based on the area of each Schottky diode, Table 6 lists the model parameters of the various transistor Schottky diodes. Figure 21 shows the Schottky diode model used for simulation.

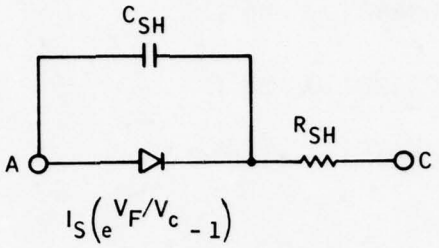


Figure 21. Schottky Diode Model

RESISTOR DESIGN

As explained in Appendix A, there are two base resistivities, high-ρ and low-ρ. Each type has its own characteristics which influence how actual resistor values are obtained. Actual resistor characteristics are listed in Table 9.

High-ρ Resistors

Typical high-ρ implanted resistors are shown in Figures 22 and 23. The resistance is largely determined by the length, x, of the high-ρ implant region. To calculate the actual resistance, the final length (x - Δx) and width, W + ΔW, after processing, must be determined. End effects cannot be ignored. A contact resistance and end resistance factor due to the low ρ diffusion must be accounted for. The number of squares of bulk high-ρ resistance is given by:

$$\square = \frac{x - \Delta x}{W + \Delta W}$$

TABLE 9. RESISTOR VALUES

Resistor	Resistance	ρ	W (μ)	x (μ)	Capacitance		Comments
					OV. (pF)	Boat (pF)	
R1	40 K Ω	high	4	544	2.4	4.24	*R24
2	7,234	special	4	1290.5	6.98	7	See text
3	951	low	4	318	3.6	8.7	*R17, 2 parallel 1902 Ω
4	40 K	high	4	554	2.4	10.12	*R18, 19
5	1 K	low	10	67.5	2.7	2.67	4 series 250 Ω } Matched
6	52.5	low	10	56	2.32	2.38	4 parallel 210 Ω } Matched
7	716	low	10	202.5	1.756	3.3	*R60
8	1.5 K	low	6	310.5	1.986	1.3	
9	951	low	4	318	3.6	8.7	*R27, 2 parallel 1902 Ω
10	1,840	high	10	49.5	0.51	0.87	
11	40 K	high	4	554	2.4	4.74	*R12, R25
12	1 K	high	10	27.5	0.35		*
13	17,566	high	10	455	3.45	3.77	
15	5,620	high	10	147	1.216	5	*R16
16	20,428	high	10	529	3.986		*
17	211	low	4	138	3.6		* 4 parallel 844 Ω
18	40,000	high	4	554	2.4		*
19	18,737	high	10	485	3.667		*
21	13,727	high	10	356	2.732	3.19	
22	16,500	high	10	427.5	3.25	3.38	
23	4,820	low	4	814	4.373	5.68	
24	1,000	high	10	27.5	0.35		*
25	2,240	high	10	59.5	0.582		*
26	8,890	high	10	231	1.825	2.08	
27	211	low	4		3.6		* 4 parallel 844 Ω
30	1,500	low	6	310.5	9.986	4.6	* R31, R36
31	1,000	low	6	205.5	1.346		
32	4,000	high	10	105	.912	†	
33	4,000	high	10	105	.912	†	
34	716	low	10	202.5	1.756		*R62

TABLE 9. RESISTOR VALUES (continued)

Resistor	Resistance	ρ	W (μ)	x (μ)	Capacitance		Comments
					OV. (pF)	Boat (pF)	
R43	2,000	high	10	53.5	.539	†	
44	110	special	41	94	2.75	†	High current
46	1 K	low	6	205.5	1.346		*
47	3,500	high	10	92	.817	†	
60	716	low	10	202.5	1.756		*
62	716 Ω	low	10	202.5	1.756		*
63	716	low	10	202.5	1.756	1.65	
64	716	high	10	202.5	1.756	1.65	
65	3,000	high	10	79	.723	†	
90	3,240	low	6	676	2.40	4.72	
91	12,150	high	10	315	2.43	2.8	
92	4.570	low	6	955	5.92	6.04	
93	3,300	high	10	87	.66	.90	
94	1,475	low	6	305	1.95	2.11	
95	122	high	10	20.5	1.8	1.94	6 parallel 732 Ω
101	1,600	low	10	111	4.09	3.56	4 series 400 Ω
102	1,600	low	10	111	4.09	3.56	4 series 400 Ω
103	100	low	10	111	4.088	3.56	4 parallel 400 Ω
104	2,800	low	6	583.5	3.8	3.44	
105	124.5	low	10	139.5	5.0	3.94	4 parallel 498 Ω
106	4,325	low	6	904	5.8	5.26	
107	265	low	10	72	.71	.74	
109	1,105	low	6	227.5	1.48	1.87	
110	100	low	10	24	.32	.37	
111	100	low	10	111	4.088	3.56	4 parallel 400 Ω
112	6,250	low	6	1308	8.18	7.35	
116	1,069	low	6	220	1.44	2.55	
118	1,670	low	6	346	2.2	2.69	
119	1,775	low	6	368	2.4	2.84	
120	4,380	low	6	915.5	5.78	7.7	* R130

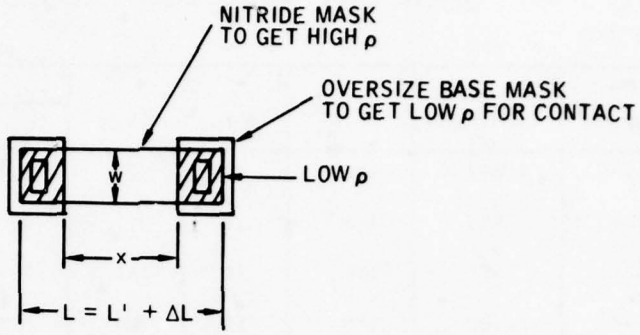
TABLE 9. RESISTOR VALUES (concluded)

Resistor	Resistance	ρ	W (μ)	x (μ)	Capacitance		Comments
					OV. (pF)	Boat (pF)	
R129	1,375	low	6	284	1.86	3.57	*, R131
130	974	low	10	277.5	2.38		*
131	591	low	10	166.5	1.47	†	
132	1,500	low	10	430	3.66	†	
133	2,100	low	10	604	5.62	†	
134	313	low	10	86	.82	.88	
135	313	low	10	86	.82	.88	
136	1,550	low	10	444.5	3.78	6.19	*, R137
137	1,910	low	6	396.5	2.55		*
138	1,910	low	6	396.5	2.55		
139	2,990 Ω	low	6	623.5	3.94	3.90	
140	1,815	low	6	376.5	2.39	2.90	
141	6,597	low	6	1381	8.8	9.98	*, R142
142	2,087	low	6	433.5	3.70		*
143	5,738	low	6	1200.5	7.64	6.68	
144	5,359	low	6	1121	7.26	8.06	*, R145, R146
145	684	low	6	139	0.98		*
146	100	low	10	24	0.324		*
147	7,800	high	10	203	1.62	1.74	
148	450	high	10	13.5	0.25	0.42	

* In boat with other resistors

† Tied to Vcc to minimize capacitance

When resistors are in parallel or series, the length, x, is for one resistor only, not the sum of individual lengths.



$\Delta x = \Delta w =$ 1.0 MASK
0.5 PHOTO PROCESS (NITRIDE)
+ 1.4 DIFFUSION
2.9 μ

$\Delta L =$ 1.0 MASK
2.1 PHOTO PROCESS (OVERLAY MASK)
+ 1.4 OUT DIFFUSION
4.5 μ

$L' = x + 2\,(3 + 3 + 2)$

Figure 22. 10-μ High-ρ Resistor Layout

The bulk resistance, R_b, is given by

$$R_b = 500 \times \square = 500 \frac{(x - \Delta x)}{W + \Delta W}$$

The contact resistance per end is given by $(125)/\ell_c$ where ℓ_c is the length of the contact after oxide cut.

The low ρ-end resistance per end of the resistor in Figure 22 is given by $(\ell_1\ 50)/W_1\ \Omega$, where ℓ_1 is the spacing from contact edge to low-ρ diffusion edge, and W_1 is the same as $W + \Delta W$.

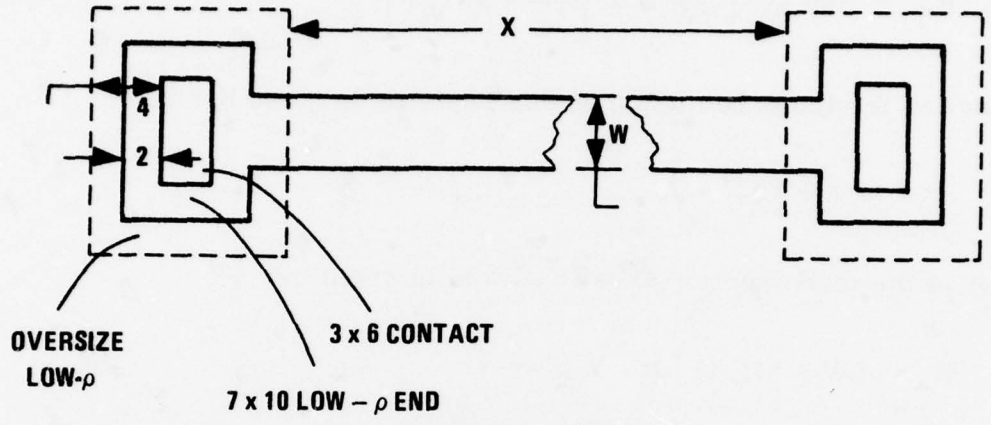


Figure 23a. 4 μ High-ρ Resistor Layout

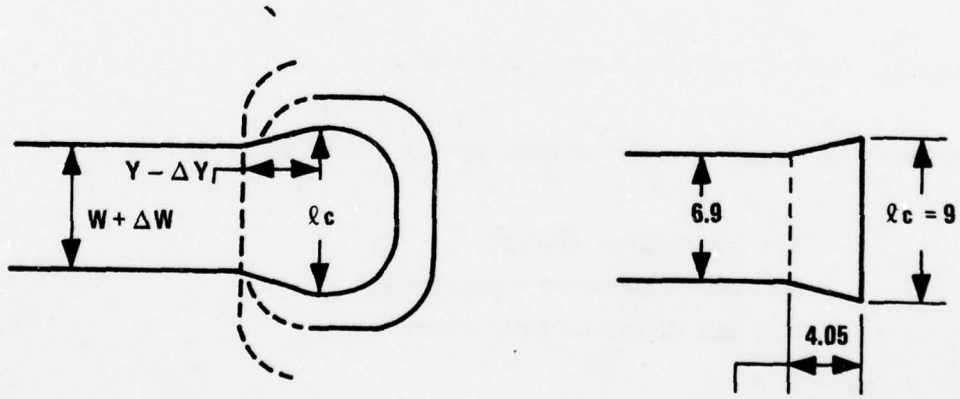


Figure 23b. 4 μ High-ρ Resistor End After Processing

Therefore, the total resistance of the resistor type shown in Figure 22 is:

$$R_T = 500 \frac{(x - \Delta x)}{(W + \Delta W)} + 2 \left[\frac{125}{\ell_c} + 50 \frac{\ell_1}{W_1} \right]$$

The equation for the capacitance of this resistor is given by:

$$C = 4.8 \times 10^{-4} \cdot A \text{ pF}$$

where A is the total junction area in μ^2 and is given by:

$$A = LW + 2(1.1)[L + W]$$

where

L = Total diffusion length = Layout dimensions + ΔL

W = Total diffusion width = W + ΔW

1.1 = Junction depth

Alternately, L is calculated as $x + 2(8 + \frac{\Delta L}{2})$.

To calculate Δx, consider the base oversize mask and low ρ:

1.0 mask size change
+ 0.5 photo process size change
+ 1.4 out diffusion both sides
$\Delta x = 2.9.$

To calculate ΔW, consider the nitride mask, and high ρ:

$$
\begin{aligned}
&1.0 \text{ mask size change} \\
&+ 0.5 \text{ photo process size change} \\
&+ 1.4 \text{ out diffusion both sides} \\
\Delta W &= 2.9.
\end{aligned}
$$

To calculate ℓ_c, the final contact width, sum up these dimensions:

$$
\begin{aligned}
&6.0 \text{ layout} \\
&+ 1.0 \text{ nominal mask change} \\
&+ 2.0 \text{ photo process change} \\
\ell_c &= 9.0\ \mu.
\end{aligned}
$$

To calculate ΔL, take the sum of the size changes for L, determined by both the nitride and oversize masks:

$$
\begin{aligned}
&1.0 \text{ mask size change} \\
&+ 2.1 \text{ photo process change on nitride} \\
&+ 1.4 \text{ out diffusion for both ends} \\
\Delta L &= 4.5\ \mu.
\end{aligned}
$$

To calculate ℓ_1, the spacing between the contact and the low-ρ diffusion edge, we must calculate the relative feature edge shifts.

$$
\begin{aligned}
3.0 &= \text{layout spacing} \\
-\ 1.5 &= \text{contact edge change, one side} \\
+\ 1.45 &= \text{low-}\rho\text{ edge change, one side} \\
\ell_1 &= 2.95\ \mu.
\end{aligned}
$$

We can now calculate the resistance and capacitance for a particular resistor layout. For the FORIC design, a layout width of 10 μ was used for most high ρ resistors. Thus, the total resistance is:

$$R_T = 500 \frac{(x - 2.9)}{12.9} + 2\left[\frac{125}{9} + \frac{2.95}{12.9} \cdot 50\right]$$

$$R_T = 38.76\,(x - 2.9) + 50.64$$

Therefore, starting with the resistor value, the layout dimension x can be determined by:

$$x = \frac{R_T - 50.64}{38.76} + 2.9$$

The spacing ℓ_1 was incorrectly estimated to be 2.0 μ, so the resistors listed in Table 9 were calculated from this equation:

$$x = \frac{R_T - 43.2}{38.76} + 2.9$$

The capacitance is now determined from the layout dimensions:

$$C = 4.8 \times 10^{-4}\,[(x + 2(8) + 4.5)\,(12.9) + 2.2(x + 20.5 + 12.9)]$$

$$= 4.8 \times 10^{-4}\,[15.1\,(x + 20.5) + 28.38]$$

$$= 0.00725\,(x + 20.5) + 0.0136 \text{ pF}$$

The length ΔL was incorrectly estimated to be 2.9, so the capacitance listed in Table 21 was calculated from this equation:

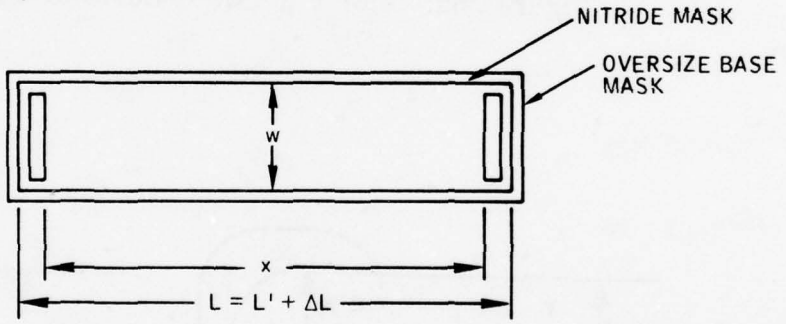
$$C = 0.00725\,(x + 18.9) + 0.0136 \text{ pF}$$

Low-ρ Resistors

Typical low-ρ resistors are shown in Figures 24 and 25. The resistance is determined by the number of squares of resistance plus contact resistance. For the resistor shown in Figure 24 there is no end resistance factor; for that in Figure 25, there is. The final length, $x - \Delta x$, and width, $W + \Delta W$, will be calculated from the Δx and ΔW shown in Figure 24.

- The number of squares is $\frac{x - \Delta x}{W + \Delta W}$.
- The bulk resistance is $50 \frac{(x - \Delta x)}{(w + \Delta w)}$.
- The contact resistance is $2 \times \frac{125\ \mu}{W_c + \Delta W_c}$.

where W_c is the layout width of the contact and $\Delta W_c = 3\ \mu$ is the total size change of the contact.



Δx = 1.0 MASK
+2.0 PHOTO PROCESS (CONTACT)
3.0μ

Δw = 1.0 MASK
2.1 PHOTO PROCESS (NITRIDE AND OVERLAY)
1.4 OUT DIFFUSION
4.5μ

$\Delta L = \Delta w$

$W = w + \Delta w$

$L' = x + 2\,(3 + 2) = x + 10$

Figure 24. 10 μ Low-ρ Resistor Layout

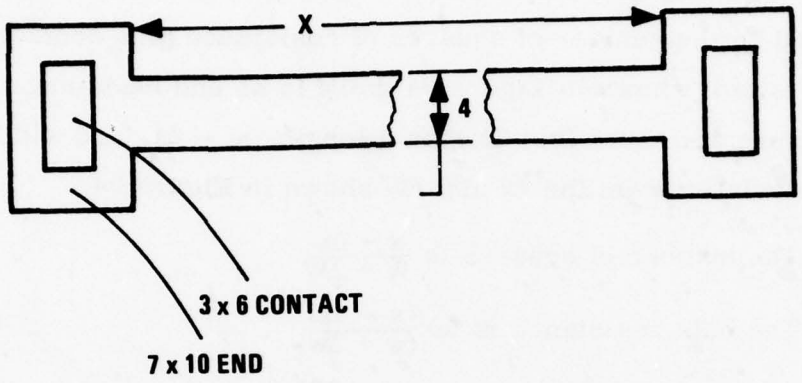


Figure 25a. 4 or 6 μ Low-ρ Resistor Layout

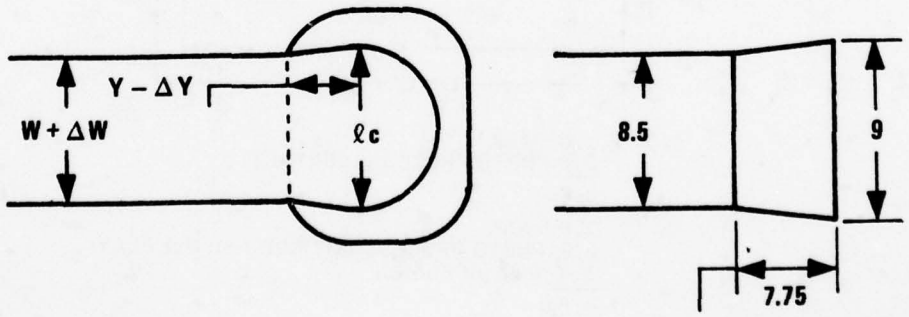


Figure 25b. 4 or 6 μ Low-ρ Resistor End after Processing

The capacitance is calculated for the low-ρ resistors of Figure 24 from

$$C = C_o \cdot A$$

where

$$C_o = 4.8 \times 10^{-4} \text{ pF}/\mu^2$$

$$A = (L + W) + 2(1.1)(L + W)$$

where

$$L = x + 10 + \Delta L$$

and

$$W = w + \Delta W = w + 4.5$$

The resistance and capacitance for 10-μ wide resistors will be calculated as a function of the layout length, x.

For w = 10 μ:

$$R = \frac{50(x - 3)}{14.5} + \frac{2(125)}{6 + 3}$$

$$R = 3.448(x - 3) + 27.78$$

Therefore,

$$x = \frac{R - 27.78}{3.448} + 3$$

The capacitance for 10-μ-wide resistors is

$$C = 4.8 \times 10^{-4} [(x + 10 + 4.5)(14.5) + 2(1.1)(x + 14.5 + 14.5)]$$

$$C = 4.8 \times 10^{-4} [x + 14.5) + 16.7 + 31.9]$$

$$C = 0.00802(x + 14.5) + 0.0153$$

High-ρ Dogbone Resistors

Dogbone resistors shown in Figures 23 and 25 have ends that increase in width because the contact size is larger than the resistor body, adding a term to the resistance equation. Using the previously derived expressions for contact resistance and resistance for the center section, the trapezoidal end section can be considered to be of average width $[W + \Delta W + \ell_c/2]$ and length $Y + \Delta Y$ as shown in Figure 23. The total resistance is:

$$R_T = \frac{x - \Delta x}{W - \Delta W} (500) + (2) \frac{125}{\ell_c} + (2) \frac{Y - \Delta Y}{(W + \Delta W + \ell_c)/2} (50)$$

Low-ρ Dogbone Resistors

Figure 25 shows the geometry used for low-ρ dogbone resistors. The trapezoidal end sections contribute to overall resistance in the same manner as for high-ρ dogbone resistors. In this case,

$$R_T = \frac{x - \Delta x}{W - \Delta W} (50) + (2) \frac{125}{\ell_c} + (2) \frac{Y - \Delta Y}{(W + \Delta W + \ell_c)/2} (50)$$

The layout dimensions for the special R2 resistor are shown in Figure 26. In the final IC layout R2 was split into two pieces to fit the chip space available. Resistance and capacitance calculations similar to the preceding calculations were performed on R2, with the results summarized in Table 9.

RESISTOR MODELS

Model for Resistors in Common Epi

The normal method for reverse biasing the p-n junction of a base resistor is to connect the n epi region (surrounding the p resistor) to the most positive potential used on the IC. Multiple resistors use their same boat (epi region). This method minimizes the isolated regions required, and, by reverse biasing to the maximum available potential, minimizes the p-n junction capacitance.

The model for a resistor in a common epi boat is shown in Figure 27. The cross section shows the resistor boat tied to the most positive potential in the circuit. The distributed capacitance is the p-n junction is lumped with half at each end.

Model for Individually Isolated Resistors

Connecting a resistor's boat to the most positive power supply voltage has the advantage of minimum p-n junction capacitance. However, this method has the disadvantage that the resistor is AC coupled to supply transients which produce undesirable extraneous noise. A method for reverse biasing

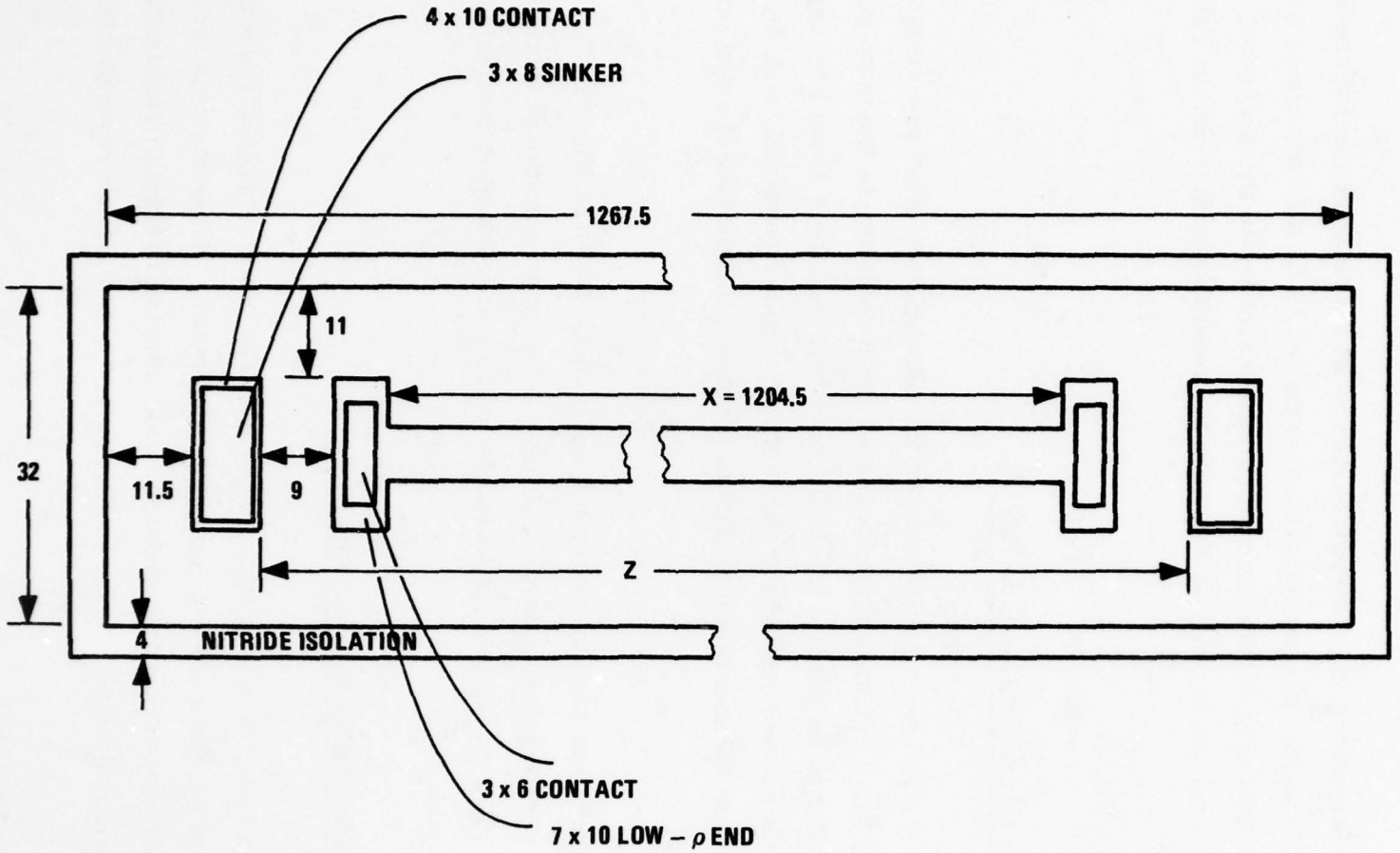


Figure 26. Special Resistor R2 Layout

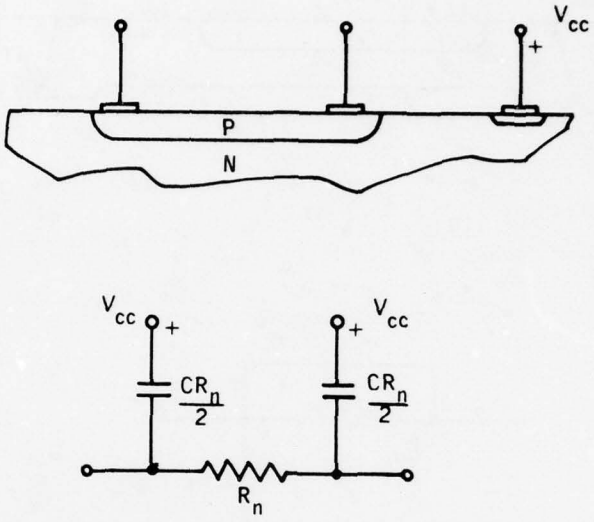


Figure 27. Model for Resistor in Common Epi

without coupling to supply variations is to connect the resistor boat to the most positive end of the resistor itself. This method usually requires a separate isolated region for each resistor.

When two or more resistors are connected together at the most positive end of each resistor, such as R12, R24, and R25 in Figure 9, they can be placed in the same boat. This biasing method was used throughout the pre-amp stages to minimize coupling to the supply voltage.

The model for a resistor in its own boat is shown in Figure 28. The cross section shows the boat tied to the most positive end of the resistor. The distributed capacitance is placed in parallel with the resistor while the boat to substrate capacitance is connected to the most positive end of the resistor.

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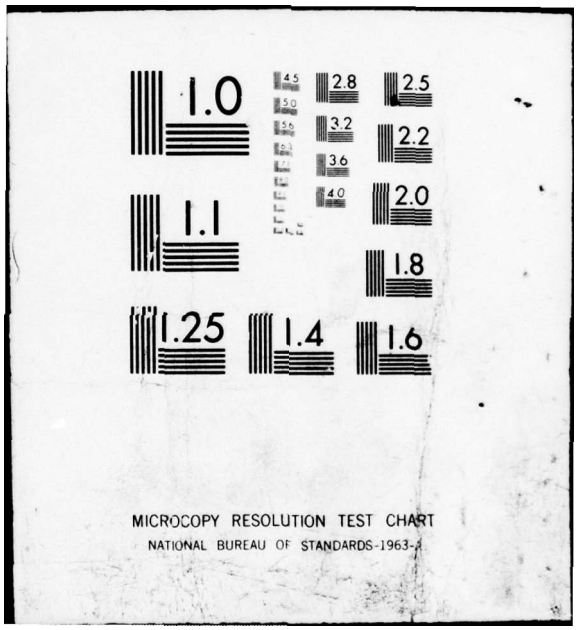
1.0
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1.25
1.4
1.6
1.8
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2.2
2.5
2.8
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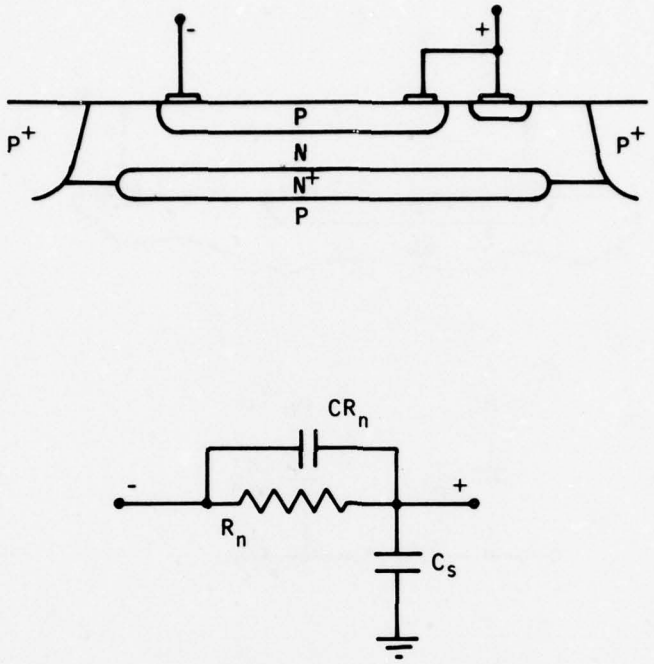


Figure 28. Model for Resistor in Separate Isolation

Model for Special Resistor R2

Another method of biasing the p-n junction of a base resistor is shown in Figure 29. The most positive end of the resistor is connected to the boat near that end and then to a positive voltage. The other end of the resistor is driven by a signal source. The other end of the boat is driven by a duplicate (or equivalent) signal source. The distributed p-n junction capacitance is lumped into four equal parts. The bias across any one of these capacitors tends to zero, and the change in bias (dv/dt) also is zero. Thus, in effect, since no current flows in the capacitor and there is no bias across it, the capacitance does not exist--i.e., no charge (q) from these capacitors will be given up or taken from the circuit containing R_n. Actually, since the

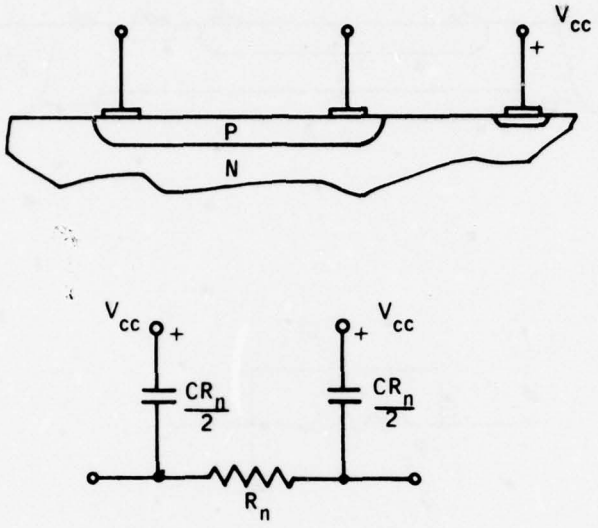
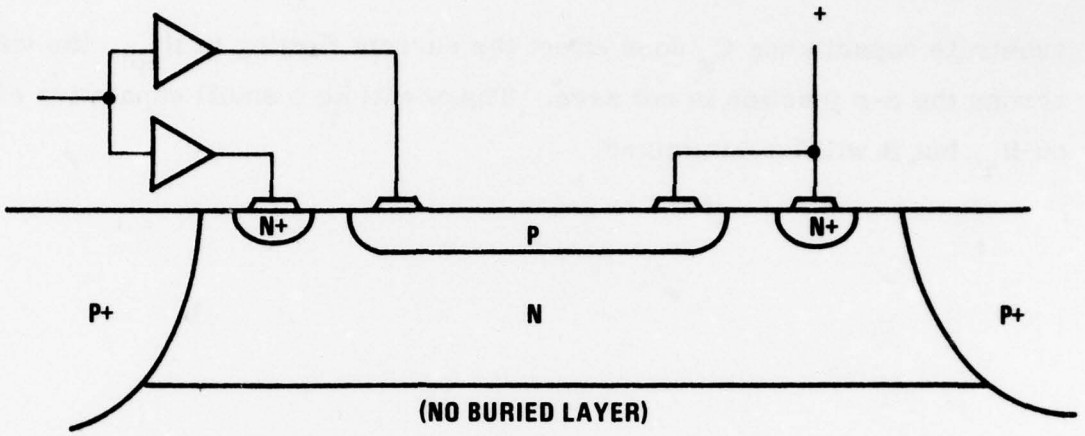


Figure 27. Model for Resistor in Common Epi

without coupling to supply variations is to connect the resistor boat to the most positive end of the resistor itself. This method usually requires a separate isolated region for each resistor.

When two or more resistors are connected together at the most positive end of each resistor, such as R12, R24, and R25 in Figure 9, they can be placed in the same boat. This biasing method was used throughout the pre-amp stages to minimize coupling to the supply voltage.

The model for a resistor in its own boat is shown in Figure 28. The cross section shows the boat tied to the most positive end of the resistor. The distributed capacitance is placed in parallel with the resistor while the boat to substrate capacitance is connected to the most positive end of the resistor.



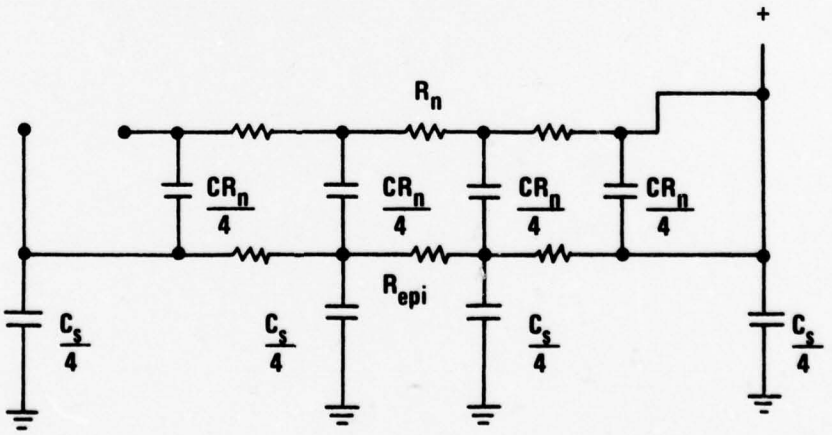


Figure 29. Model for Special Resistor R2

substrate capacitance C_s does effect the current flowing in R_{epi}, the voltage across the p-n junction is not zero. There will be a small capacitive effect on R_n, but it will be minimized.

SECTION VI

TESTING AND PACKAGING

FORIC TEST PLAN

A test plan is a description of a device's performance characteristics that can be programmed into an automatic tester to ensure that the device will operate as specified. The test plan must be usable for testing devices in both of their primary forms, which are wafers and packages.

FORIC devices were tested three times before shipping. First, the devices were tested in wafer form on the automatic tester to select those die to be packaged. Because the die must be probed to make electrical contact when they are in wafer form, long lines to/from the automatic tester limit the type of test that can be made. Only DC conditions are tested when the device is in wafer form. The AC tests are made on packaged die only, because only after packaging can the input and output impedances be easily controlled.

Packaged chips were tested after environmental screens, except burn-in, had been performed (see Table 10). At that time, all DC and AC tests were performed to select the devices to be burned in. After burn-in, the devices were tested a third and final time just prior to shipping. The AC tests were performed in the lab with a special fixture shown in Figure 30. The automatic tester did not have the capability to supply the small input currents accurately; manual testing of some parameters was necessary.

TABLE 10. TEST PLAN LISTING FOR FORIC

Test No.	Pin / Pad / Test	1 F Vcc	2 E Output	3 G GND	4 C Coup. C	5 B Coup. B	6 H 1.7 V	7 D Signal	8 G GND	9 A AGC	10 K By-pass	11 J 3.9 V	12 L Band Gap	Notes	Min.	Max.	Units
1-12	Probe contact	±1 mA MV	Force ±1 mA through each pin one at a time, with all other pins at GND.											Note 1		12.01	volts
13	1.7 V regulator output	5.5 V	Open	GND	Tied together		0.5 µf MV	10 µA	GND	0.5 µf Open	Open	0.5 µf	Open	Note 2 Note 3	1.85 1.65 1.43	1.95 1.74 1.53	volts
14	1.7 V regulator output	5.0 V	Open	GND			0.5 µf MV	10 µA	GND	0.5 µf Open	Open	0.5 µf	Open		1.85 1.64 1.43	1.95 1.74 1.53	volts
15	1.7 V regulator output	4.5 V	Open	GND			0.5 µf MV	10 µA	GND	0.5 µf Open	Open	0.5 µf	Open		1.85 1.64 1.43	1.95 1.74 1.53	volts
16	3.9 V regulator output	5.5 V	Open	GND			0.5 µf	10 µA	GND	0.5 µf Open	Open	0.5 µf	Open	Same limits for all temp.	3.83	4.1	volts
17	3.9 V regulator output	5.0 V	Open	GND			0.5 µf	10 µA	GND	0.5 µf Open	Open	MV	Open	Same limits for all temp.	3.83	4.1	volts
18	3.9 V regulator output	4.5 V	Open	GND			0.5 µf	10 µA	GND	0.5 µf Open	Open	MV	Open	Same limits for all temp.	3.83	4.1	volts
19	Measure AGC voltage	5.0 V	Open	GND			0.5 µf	1 µA	MV	0.5 µf Open	Open	0.5 µf	Open		1.85 1.64 1.43	2.05 1.84 1.63	volts
20	Icc max "1" input	5.5 V MC	-400 µA	GND			0.5 µf	10 µA	GND	Force -20 mV	Open	0.5 µf	Open		30 30 30	47 45 44	mA
21	Icc max "0" input	5.5 V MC	16 mA	GND			0.5 µf	1 µA	GND	Force -20 mV	Open	0.5 µf	Open		30 30 30	47 45 44	mA
22	Overvoltage "1" input	7 V MC	-400 µA	GND			0.5 µf	10 µA	GND	Force -20 mV	Open	0.5 µf	Open		40 40 40	55 60 55	mA

TABLE 10. TEST PLAN LISTING FOR FORIC (concluded)

Test No.	Pin / Pad / Test	1 F Vcc	2 E Output	3 G GND	4 C Coup. C	5 B Coup. B	6 H 1.7 V	7 D Signal	8 G GND	9 A AGC	10 K By-pass	11 J 3.9 V	12 L Band Gap	Notes	Min.	Max.	Units
23	Overvoltage "0" input	7 V MC	16 mA	GND	Tied together		0.5 µf	1 µA	GND	Force -20 mV	Open	0.5 µf	Open		40 40 40	55 60 55	mA
24	Shorted output current	5.5 V	GND MC	GND			0.5 µf	10 µA	GND	Force -20 mV	Open	0.5 µf	Open	Same limits for all temp.	-20	-55	mA
25	Shorted output current	4.5 V	GND MC	GND			0.5 µf	10 µA	GND	Force -20 mV	Open	0.5 µf	Open	Same limits for all temp.	-20	-55	mA
26	Maximum input current	5.5 V	Open	GND			0.5 µf	1 mA MV	GND	Force -20 mV	Open	0.5 µf	Open	Same limits for all temp.	1.5	1.8	volts
27	Minimum "1" output	4.5 V	-400 µA MV	GND			0.5 µf	10 µA	GND	Force -20 mV	Open	0.5 µf	Open	Same limits for all temp.	2.7	4.0	volts
28	Maximum "0" output	4.5 V	16 mA MV	GND			0.5 µf	1 µA	GND	Force -20 mV	Open	0.5 µf	Open	Same limits for all temp.	0.1	0.4	volts
29	AGC ratio "0"	5.0 V		GND			MVD	Open	GND	+ MVD	Open	0.5 µf	Open	Same limits for all temp.	0.06	0.10	volts
30	AGC ratio "1"	5.0 V		GND			MVD	500 µA	GND	+ MVD	Open	0.5 µf	Open	Same limits for all temp.	-0.5	-0.3	volts
31	Band gap	5.5 V		GND			MVD	1 µA	GND	Force -20 mV	Open	0.5 µf	Open	Same limits for all temp.	0	0.03	volts
32	Band gap	5.0 V		GND			MVD	1 µA	GND	Force -20 mV	Open	0.5 µf	Open	Same limits for all temp.	1.22	1.28	volts
33	Band gap	4.5 V		GND			MVD	1 µA	GND	Force -20 mV	Open	0.5 µf	Open	Same limits for all temp.	0	0.03	volts

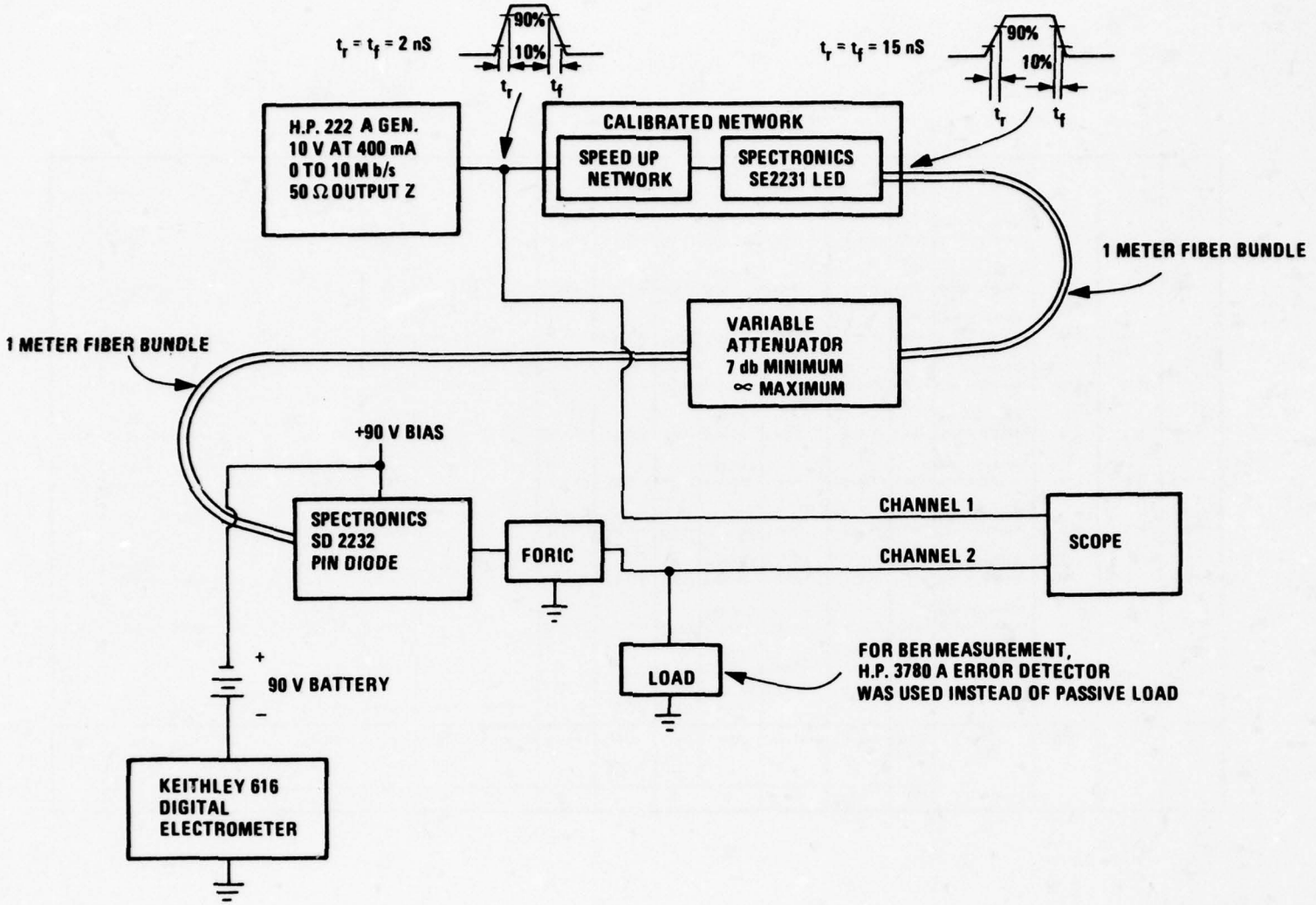


Figure 30. AC Test Setup for FORIC

The following test plan has been implemented on an automatic tester that was used as described above. The test plan contains DC tests 1 through 33. A description of the tabulated test plan in Table 10 is provided to explain the purpose of the test and to make it easier to correlate the test plan with the device specification. AC tests are covered in the following description.

DC TESTS

Notes for Table (Test Plan Listing)

Note 1: MV = Measure Voltage

MC = Measure Current

MVD = Measure Voltage Difference

Note 2: When three limit values are given, the top one is for -55° C, the middle one for +25° C, and the bottom one for +150° C junction temperature.

Note 3: Tie pins 4 and 5 together for all tests except probe contact tests.

Tests 1 Through 12: Probe Contact

There are 12 probing pads. To insure the probe is making contact to a given pad and that there is no opening from pad to substrate, a $\pm$1 mA current is forced through each pad, one at a time, and the voltage at that pad relative to ground is measured while the other 11 pads are tied to ground. The voltage should always be less than two diode drops from substrate (ground).

- Force $\pm$1 mA in each pad to ground.
- Limit the supply to | 5 | V.
- Measure < | 2 | volts at all temperatures.

Tests 13 Through 15: 1.7 V Regulator Output

The internal 1.7 V regulator is tested over voltage and temperature range. The 1.7 V should be constant with voltage but should exhibit a -2.15 mV/° C temperature dependence. The 10 μA forced into the signal input should prevent noise from causing oscillation.

- Force 10 μA in pin 7, limit voltage to 2.4 V.
Force Vcc = (Limit at 70 mA)		5.5 V	5.0 V	4.5 V
Measure at -55° C pin 6	=	1.90 $\pm$ 0.05 volts	Same	Same
Measure at +25° C pin 6	=	1.70 $\pm$ 0.04 volts	Same	Same
Measure at +150° C pin 6 (T_j)	=	1.48 $\pm$ 0.05 volts	Same	Same

Tests 16 Through 18: 3.9 V Regulator Output

The internal 3.9 V regulator is tested over voltage and temperature range. The 3.9 V should be constant with voltage and temperature.

- Force 10 μA in pin 7, limit voltage to 2.4 V.
Force Vcc = (Limit at 70 mA)		5.5 V	5.0 V	4.5 V
Measure at -55° C or +25° C or +150° C (T_j) pin 11	=	3.90 + 0.2 volt - 0.07 volt	Same	Same

Test 19: Measure AGC Voltage

This test is actually only a calibration of the AGC voltage to allow the output to be switched on and off by applying two known currents to the input. Since the coupling capacitor is shorted, the receiver is essentially DC coupled and therefore follows DC input current levels.

- Apply 5 V to Vcc.
- Force 1 μA into pin 7 (input), limit voltage to 2.4 V.
- Measure AGC voltage on pin 9 =

-55°C	+25°C	+150°C	
1.95 $\pm$ 0.1	1.74 $\pm$ 0.1	1.53 $\pm$ 0.1	volts

- Calculate (AGC voltage - 20 mV) at each temperature.

Decreasing the AGC voltage by 20 mV with a known input current has the effect of disabling the AGC and changing the pre-amp gain by shunting all the input current into the AGC. Since the receiver is DC coupled at this time, the output switches off. Starting with a known current overrides the noise generated on the input that would randomly switch the output. To switch the output on requires a higher level current input. For the remaining tests, applying 1 μA while forcing (AGC voltage - 20 mV) turns the output off and then applying 10 μA to the input turns the output on.

Tests 20 and 21: I_{CC} Maximum

This test insures there are no excessively leaky junctions or direct shorts that load the power supply above the normal current drain. The total current

drain is independent of the logic state but it is tested in both states in an attempt to reverse bias all junctions.

Force Logic "1" Means--

- Force (AGC voltage - 20 mV) on pin 9, limit current to 2 mA.
- Force 10 μA in pin 7 (input), limit voltage to 2.4 V.
- Force -400 μA in pin 2, limit voltage to 2.7 V.

Force Logic "0" Means--

- Force (AGC voltage - 20 mV) on pin 9, limit current to 2 mA.
- Force 1 μA in pin 7 (input), limit voltage to 2.4 V.
- Force 16 mA in pin 2, limit voltage to 1 V.
- Apply Vcc = 5.5 V, limit at 70 mA.
- Force logic "1", measure current (I_{cc}) into pin 1.
- Force logic "0", measure current (I_{cc}) into pin 1.

T_j =	-55° C	+25° C	+150° C	
I_{cc} Maximum =	47	45	44	mA
I_{cc} Minimum =	30	30	30	mA

Tests 22 and 23: Overvoltage

This test stresses the junctions to weed out the weak ones. The die is not required to operate at Vcc = 7 V but both logic states are tested to bias all junctions under stress.

- Apply Vcc = 7 V, limit at 70 mA.
- Force logic "1" (same as for tests 20 and 21), measure I_{cc} into pin 1.
- Force logic "0" (same as for tests 20 and 21), measure I_{cc} into pin 1.

	-55° C	+25° C	+150° C	
I_{cc} Maximum =	55	60	55	mA
I_{cc} Minimum =	40	40	40	mA

Tests 24 and 25: Shorted Output Current

This test checks the TTL output current limiting resistor and high level drivers. The maximum shorted output current is worst case at Vcc = 5.5 V and the minimum shorted output current is worst case at Vcc = 4.5 V as both voltages must be checked.

- Force Vcc = 5.5 V, limit current to 70 mA or
- Force Vcc - 4.5 V, limit current to 70 mA.
- Force (AGC voltage - 20 mV) on pin 9, limit current to 2 mA.
- Force 10 μA in pin 7 (input).
- Force ground on pin 2.
- Measure current from pin 2 only into ground.
- At all temps it should be -20 mA minimum and -55 mA maximum.

Test 26: Maximum Input Current

This test checks the Schottky clamp on the input transistor and the AGC reaction time. The AGC's main function is to allow the input to sink current in excess of the few microamperes required for base current on the input without saturating the input stage. If a 0.5 μF capacitor is tied to the AGC pad (pin 9), the time constant for the AGC reaction becomes long (> 10 μ/sec) and any input current must go through the Schottky clamp. If the Schottky is bad, or the AGC is shorted out or not functioning correctly, the input cannot sink 1 mA without exceeding the test voltage limit. To insure that the AGC will not influence the input voltage, the measurement must be taken < 100 μ/sec after the 1 mA is applied.

- Apply Vcc - 5.5 V, limit to 70 mA.
- Force 1 mA into pin 6.
- Measure voltage on pin 6.
- Voltage on pin 6 = min/1.6, max/2.0 at any temperature.
- Force (AGC voltage - 20 mV) on pin 9, limit current to 2 mA.

Tests 27 and 28: Minimum and Maximum Output Voltage

This test insured correct output levels for the standard TTL totem pole output.

- Apply Vcc = 4.5 V, limit to 70 mA.
- Force logic "1".

- Measure voltage on pin 2 = 2.7 V minimum, 4.0 V maximum at all temperatures.
- Force logic "0".
- Measure voltage on pin 2 = 0.1 V minimum, 0.4 maximum at all temperatures.

Tests 29 and 30: AGC Circuit

Tests up to this point have forced the output state by effectively disabling the AGC circuit. This test determines if the AGC is working. Under nominal conditions, the AGC voltage should be 80 mV higher than the +1.7 V regulator output with no current in the input. At this point, the gain is maximum. Applying 500 μA changes the gain to minimum.

- Apply 5 V to Vcc.
- With pin 7 (input) open, measure voltage difference pin 9 +, pin 6 - 0.08 ± 0.02 V.
- Force 500 μA in pin 7 (input), limit voltage to 2.4 V.
- Measure voltage difference pin 9 +, pin 6 - -0.4 ± 0.1 V.

Tests 31 Through 33: Data Collection on Band Gap Voltage

This test primarily collects data to help determine process run variation limits.

- Force Vcc = 5.5 V.
- Measure pin 12.

- Force Vcc = 5.0 V.
- Measure pin 12 - 1.25 $\pm$ 0.03 volts.
- Force Vcc = 4.5 V.
- Measure pin 12.
- Calculate

a)	difference in band gap voltage between Vcc = 5.5 V and Vcc = 5.0 V.	0.03 V maximum at 25° C
b)	difference in band gap voltage between Vcc = 5.0 V and Vcc = 4.5 V.	0.03 V maximum at 25° C

AC TESTS

Because of the automatic tester limitation on accuracy of supplying a 250 nA, 10 Mb/sec signal, a special test fixture shown in Figure 30 was constructed to perform the AC tests.

The total length of the fiber bundle connecting the LED to the PIN diode is < 2 m. Therefore, dispersion was neglected and the input rise/fall time of the power to the PIN diode was assumed to be equal to the calibrated Spectronics SE2231 LED output of 15 ns.

With 90 V bias on the Spectronics SD2232 PIN diode, its rise/fall time is < 1 ns. This was neglected and the signal current into the FORIC was assumed to have a 15 ns, 10 to 90 percent rise/fall time.

The Keithley electrometer was used to measure the average current value in the PIN diode. All measurements were made with square wave signals so that the digital meter reading was one-half the peak-to-peak signal current.

The load for measuring the rise/fall times and delay is the standard 5400 series TTL load shown in Figure 5. For measuring the BER, a different load was used. The H. P. Error Detector has an input impedance of 50 Ω. The FORIC output was not designed to drive a 50 Ω load; instead a TTL buffer was used to couple the FORIC output into this instrument. The TTL package had six inverters, and all six inputs were tied together to simulate the standard load.

FORIC BURN-IN PLAN

The burn-in specification is Mil-Std-883, Method 1015, Condition B. This standard states that the parts shall undergo at least 168 hours (seven days) of 125° C ambient temperature under active conditions. The object of the burn-in is to temperature-stress the parts to "weed" out the early failures due to marginal junctions, wire bonds, etc.

The overall block diagram of the burn-in setup is shown in Figure 31. The logic board designed to operate the parts during burn-in is shown in Figure 32 and the device board wiring diagrams for the 14-pin DIP and TO-100 are shown in Figures 33 and 34.

On each device burn-in board there are 120 devices, 20 columns by six rows. Since the FORIC has only one input, only 12 driver gates (see Figure 31)

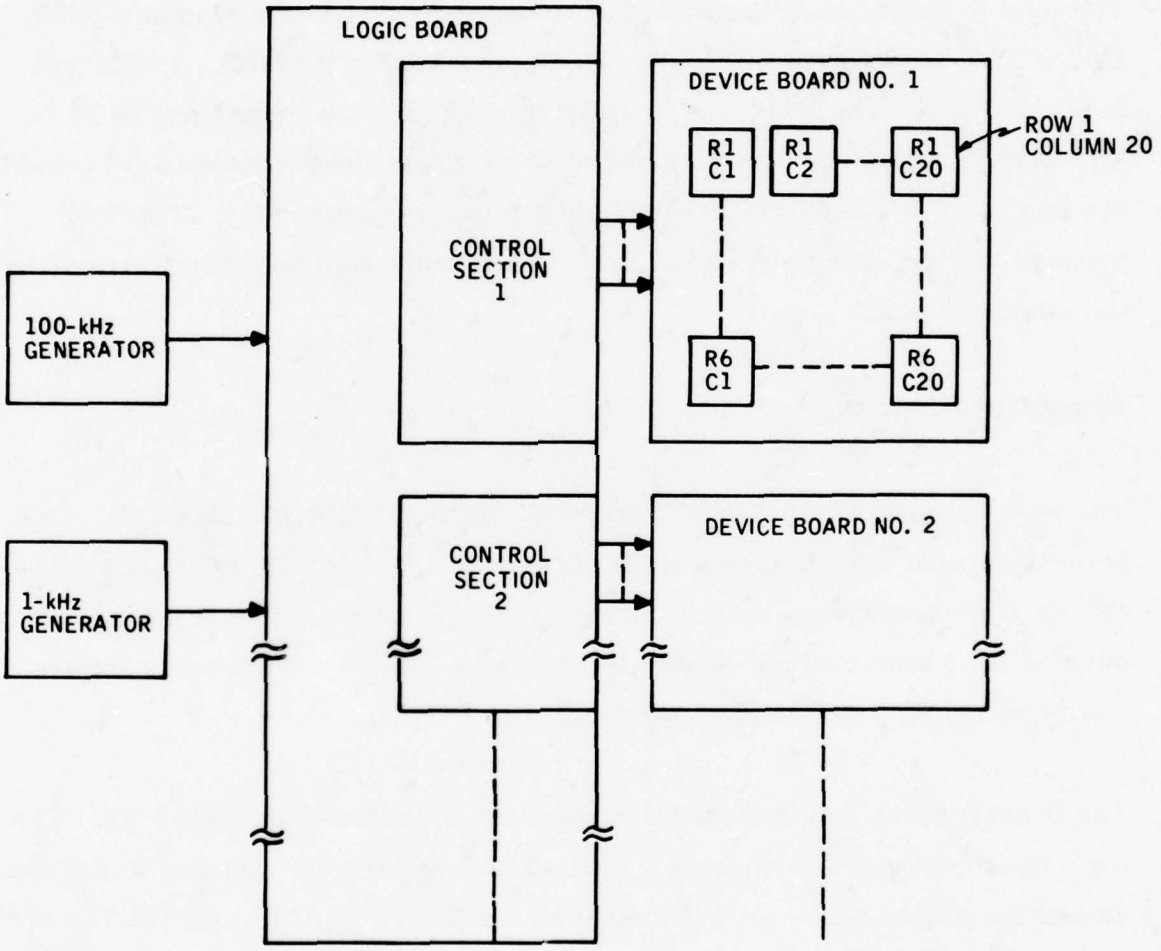


Figure 31. Burn-In Setup Block Diagram

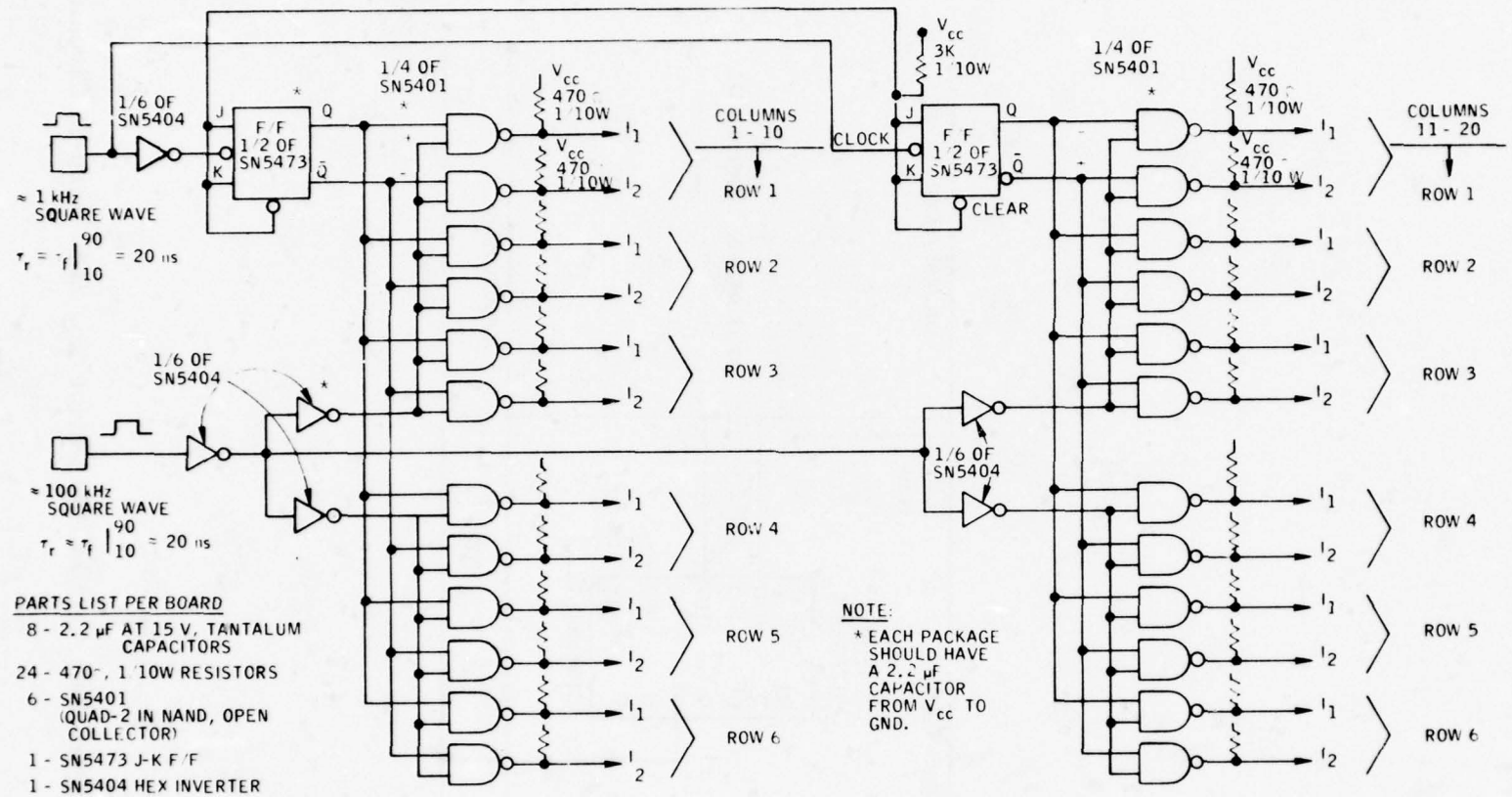


Figure 32. Control Circuits for FORIC Burn-In Board

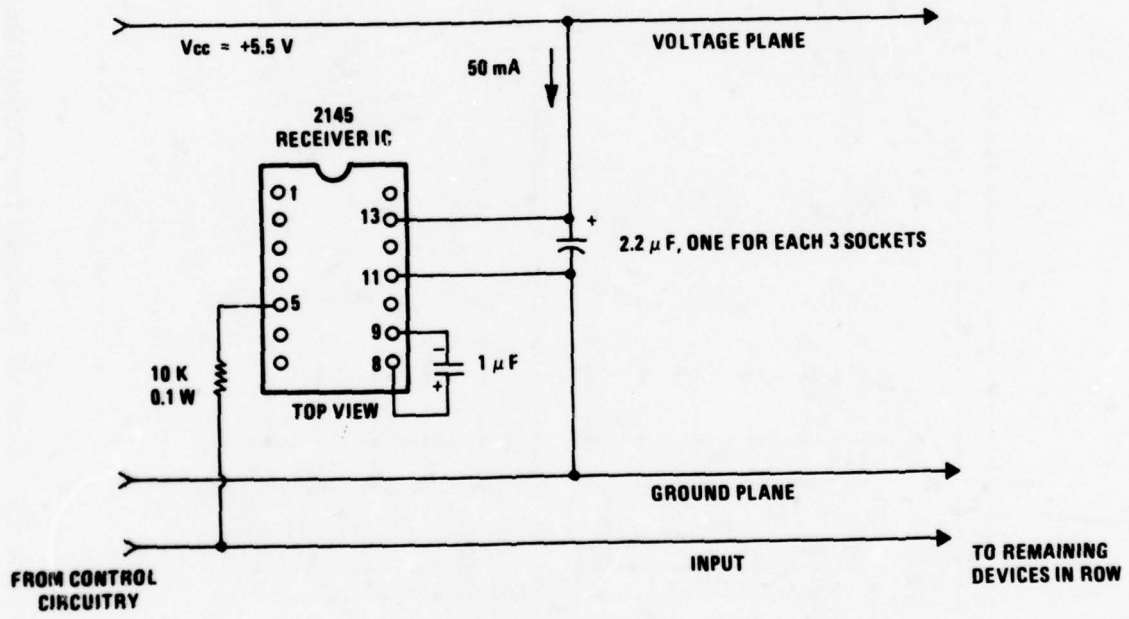


Figure 33. 14-Pin DIP Device No. 2145 Burn-In Circuit

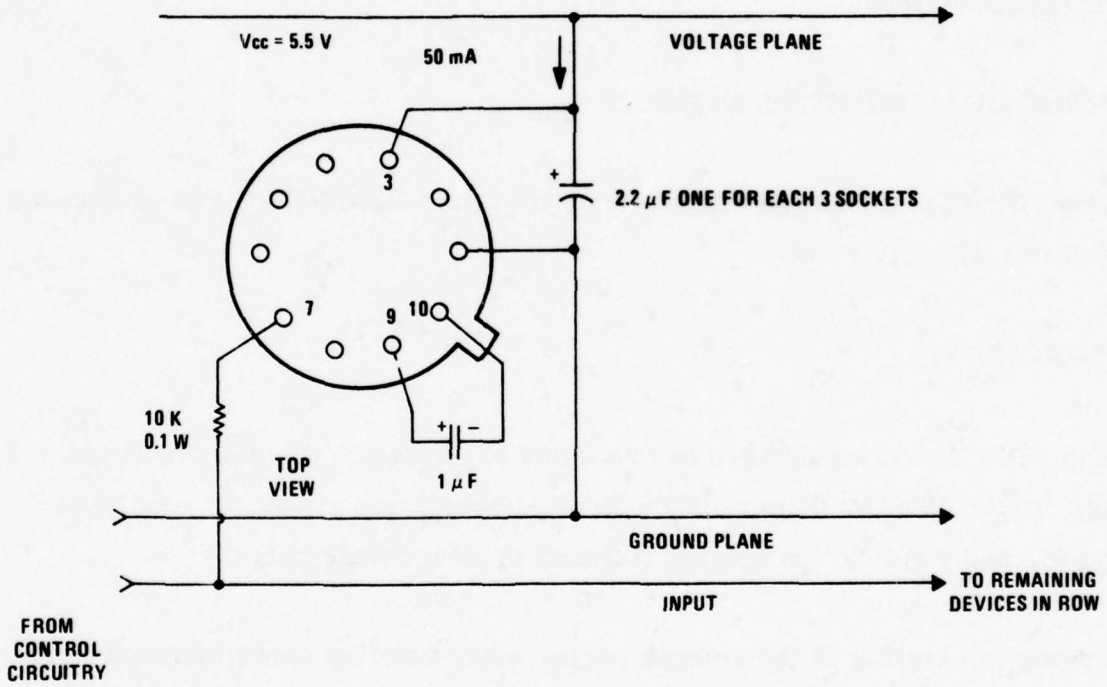


Figure 34. 10-Pin TO-100 Device No. 2145 Burn-In Circuit

are required. An open collector-type driver was used so that the inputs to the FORIC would see the maximum voltage transition that they would be subjected to under worst-case operating conditions.

The FORIC coupling capacitor package pins were shorted so that the FORIC operates like a DC coupled receiver. The idea of the control logic is to switch each FORIC at a 100-kHz rate during the burn-in process to weed out marginal devices.

FORIC QUALIFICATION PLAN

The FORIC qualification plan is written around Mil-Std-883 and is detailed in Table 11.

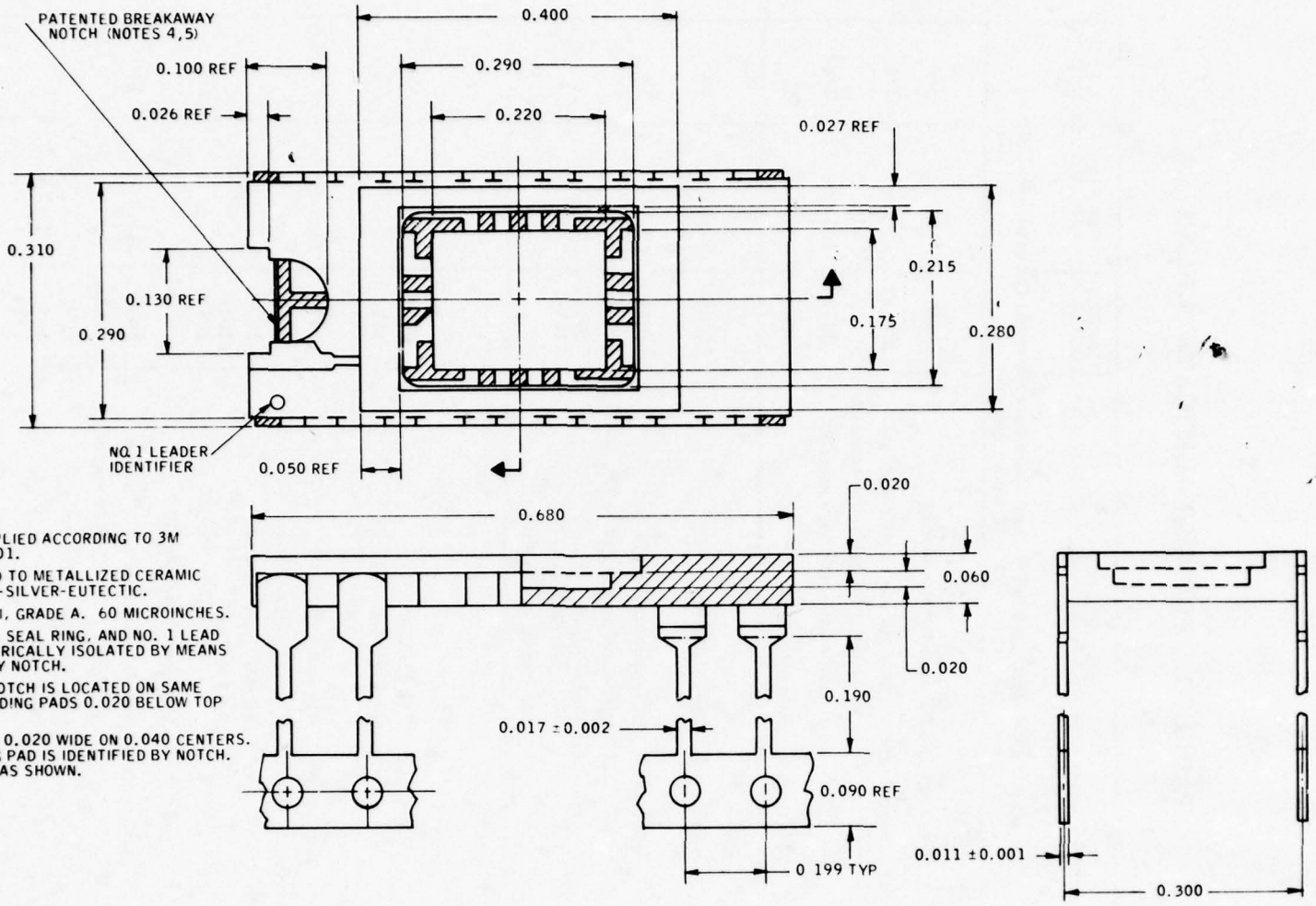
PACKAGING

The FORICs were packaged in two types of packages: 14-pin DIP (Figure 35) and 10-pin TO-100 (Figure 36). Both packages are standard, available types, and required no special fixtures or new development.

During the testing of the sample parts, many bonding configurations were attempted to determine the effects of floating or grounding the die bond area. It was determined that best performance was achieved when the die bond area (TO-100 header, 14-pin DIP cavity) of the package was connected to ground at the package pin used for external ground. The TO-100 header and can were tied to ground, as was the 14-pin DIP lid. Significant differences in performance were observed during testing with the lid connected to ground or floating.

TABLE 11. FORIC QUALIFICATION PLAN

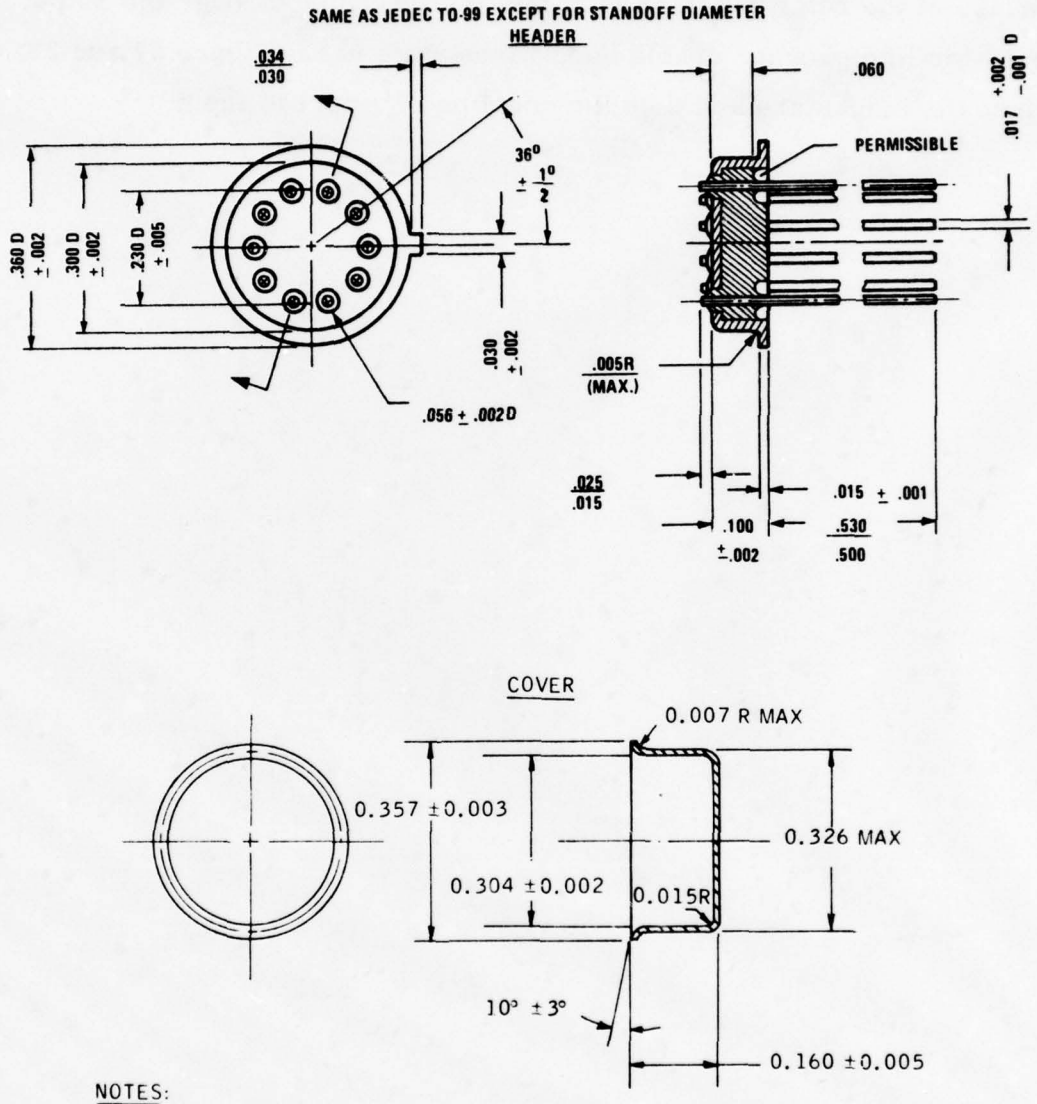
Group/Subgroup		Method	Condition	LTPD
• Group A:				
Do all per 883, Method 5005.3 Lot Tolerance Percent Defective (LTPD) = 10 all subgroups				
• Group B:				
Subgroup 1.	Physical Dimensions	2016		2/0
Subgroup 2.	a) Resistance to solvents	2015		3/0
	b) Internal visual and mechanical		Delete	
	c) Bond strength (post-seal)	2011	1.5 gm	3/0
Subgroup 3.	Solderability	2003		15
• Group C:				
Subgroup 1.	Operating life	1005	+125 C 1000 hr	10
Subgroup 2.	Temperature cycle	1010	C	15
	Constant acceleration (Y_1 only)	2001	D	
	Seal - Fine Gross	1014 1014		
	Electrical end points			
• Group D:				
Subgroup 1.	NO			
Subgroup 2.	Lead integrity	2004	B_2	2/0
	Seal - Fine Gross	1014 1014		
Subgroup 3.	Thermal shock	1011	B	15
	Temperature cycle	1010	C	
	Moisture resistance	1004		
	Seal - Fine Gross	1014 1014		
	Electrical end points			
Subgroup 4.	Mechanical shock	2002	B	15
	Vibration, variable frequency	2007	A	
	Constant acceleration	2001	E (Y_1 only)	
	Seal - Fine Gross	1014 1014		
	Electrical end points			
Subgroup 5.	Salt atmosphere		Delete	



NOTES:

1) PACKAGE SUPPLIED ACCORDING TO 3M SPEC. S-90-001.
2) LEADS BRAZED TO METALLIZED CERAMIC USING COPPER-SILVER-EUTECTIC.
3) GOLD: TYPE III, GRADE A. 60 MICROINCHES.
4) THE CHIP PAD, SEAL RING, AND NO. 1 LEAD MAY BE ELECTRICALLY ISOLATED BY MEANS OF BREAKAWAY NOTCH.
5) BREAKAWAY NOTCH IS LOCATED ON SAME LEVEL AS BONDING PADS 0.020 BELOW TOP SURFACE.
6) BONDING PADS 0.020 WIDE ON 0.040 CENTERS. NO. 1 BONDING PAD IS IDENTIFIED BY NOTCH. CORNER PADS AS SHOWN.

Figure 35. 14-Pin Ceramic Dual In-Line Package

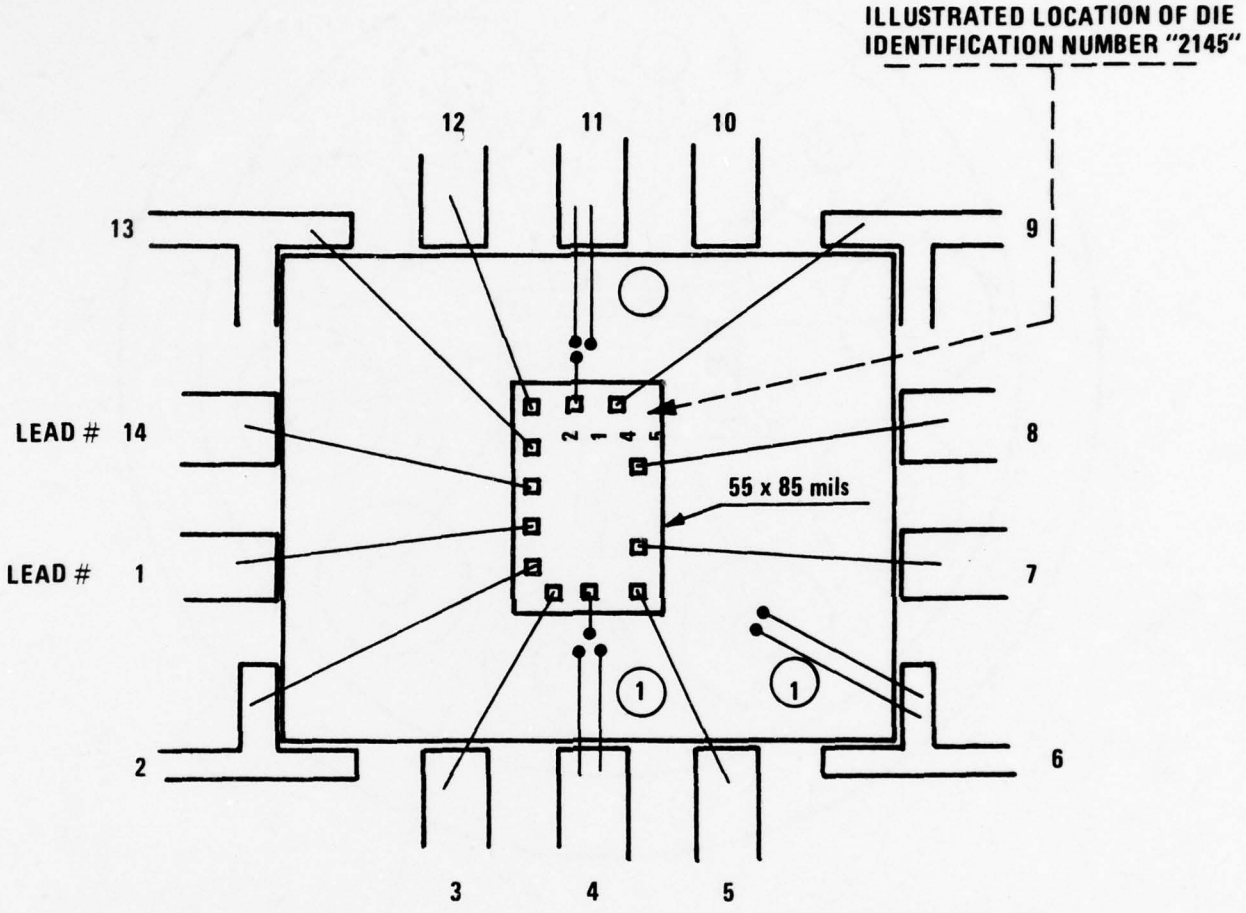


NOTES:

1) FINISH: GOLD PLATE, 80 MICROINCHES (MINIMUM) OVER ALL HEADER SURFACES BY BETA METHOD.
2) COVER MATERIAL: 0.012 GRADE A NICKEL, TYPE 200.
3) MATERIAL: BASE AND PINS - KOVAR.
4) GLASS FEED-THROUGHS TO BE OPAQUE.
5) WIRE BOND SURFACE FLAT WITHIN 0.001 FOR 0.012 DIA. MIN.

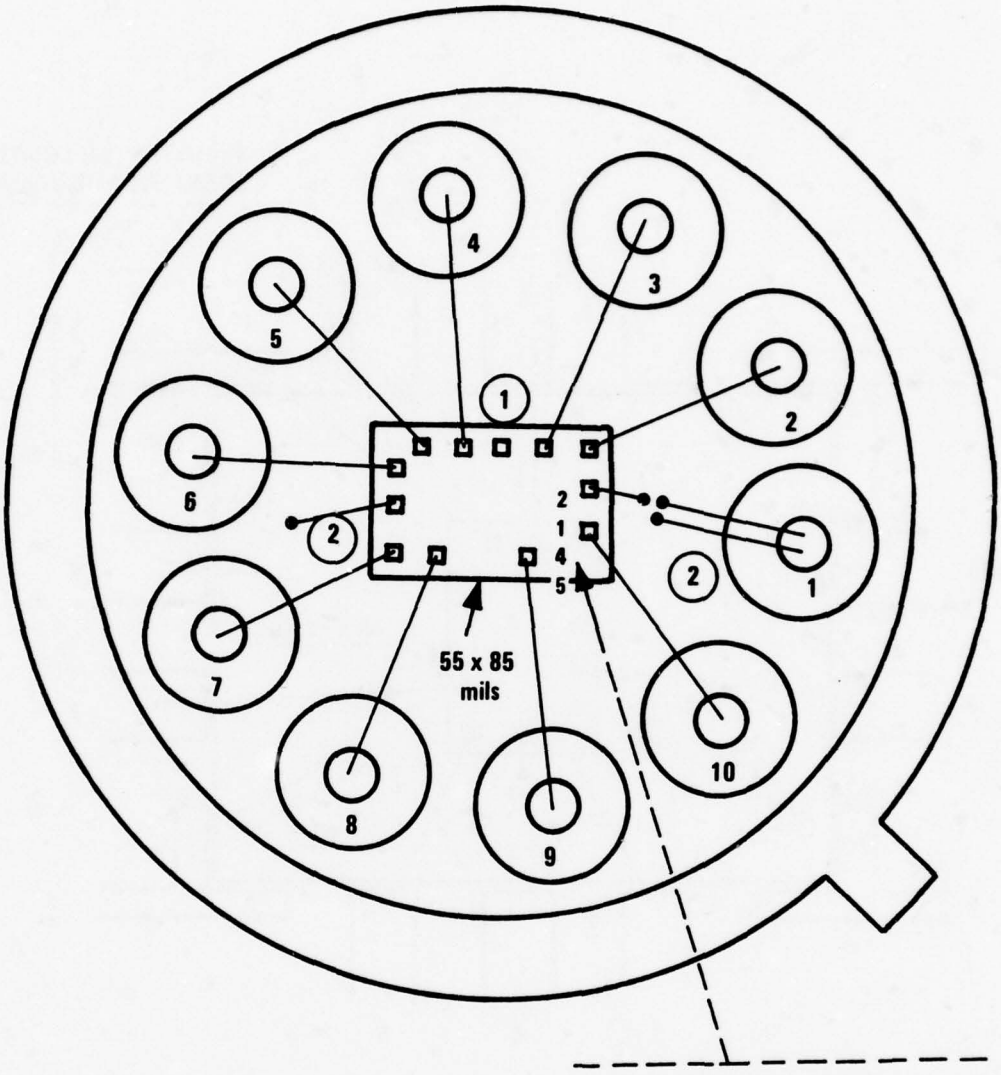
Figure 36. 10-Pin TO-100 Can

Because of the relatively high currents that can flow through the output transistor into ground, double bond wires were used (Figure 37 and 38) to reduce the inductance and thus the coupling of output to input.



(1) CONNECT PACKAGE CAVITY TO PINS 4, 6, 11 WITH TWO 1 mil WIRES EACH. KEEP BOND WIRES FROM DIE TO CAVITY AND CAVITY TO PACKAGE PINS AS SHORT AS POSSIBLE.

Figure 37. 14-Pin DIP Bonding Diagram



(1) DO NOT BOND TO THIS PAD.

(2) CONNECT PACKAGE HEADER TO PIN 1 WITH TWO 1 mil WIRES. KEEP BOND WIRES FROM DIE TO HEADER AND HEADER TO PACKAGE PINS AS SHORT AS POSSIBLE.

Figure 38. 10-Pin TO-100 Bonding Diagram

APPENDIX A

ADVANCED BIPOLAR PROCESS DESCRIPTION

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ADVANCED BIPOLAR PROCESS DESCRIPTION

The Honeywell Advanced Bipolar Process I (ABP-I) is the current standard bipolar process used for all internal Honeywell needs. Devices built using this process are used in Honeywell's large and small computers, and in various commercial and industrial sensor and control electronics, as well as classified military applications.

A brief description of the processing sequence follows. The cross-sectional views of Figure A-1 show the various diffused and implanted regions and the oxide layers used to control the etching and junction formations. The top views of Figure A-2 show the actual masks used to obtain the profiles shown in Figure A-1. Although the processing steps allow for other components (resistors, diodes, etc.) to be formed at the same time in the surface of the same wafer, both figures show only a single transistor for clarity.

The processing begins by oxidizing the surface of a polished P-type wafer to form a masking oxide layer. The first mask (buried layer, Figure A-2.1) is used to define the pattern in the oxide layer. Then the N^+ dopant is diffused into the wafer to form the buried layer (Figure A-1.1). A lightly doped N epitaxial layer (epi) is then grown and a thin layer of silicon dioxide (SiO_2) grows on top of it while the N^+ Buried Layer diffuses up into it (Figure A-1.2). The silicon nitride (Si_3N_4) is then grown on top of the SiO_2, and the second mask is used to etch the patterns that will become the self-aligned isolation, sinker, and base regions (Figures A-1.3, A-2.2). In older processes, these three regions were defined with separate patterns. Since all three regions are defined by the same pattern, higher-performance (less capacitance) and higher-density transistors result.

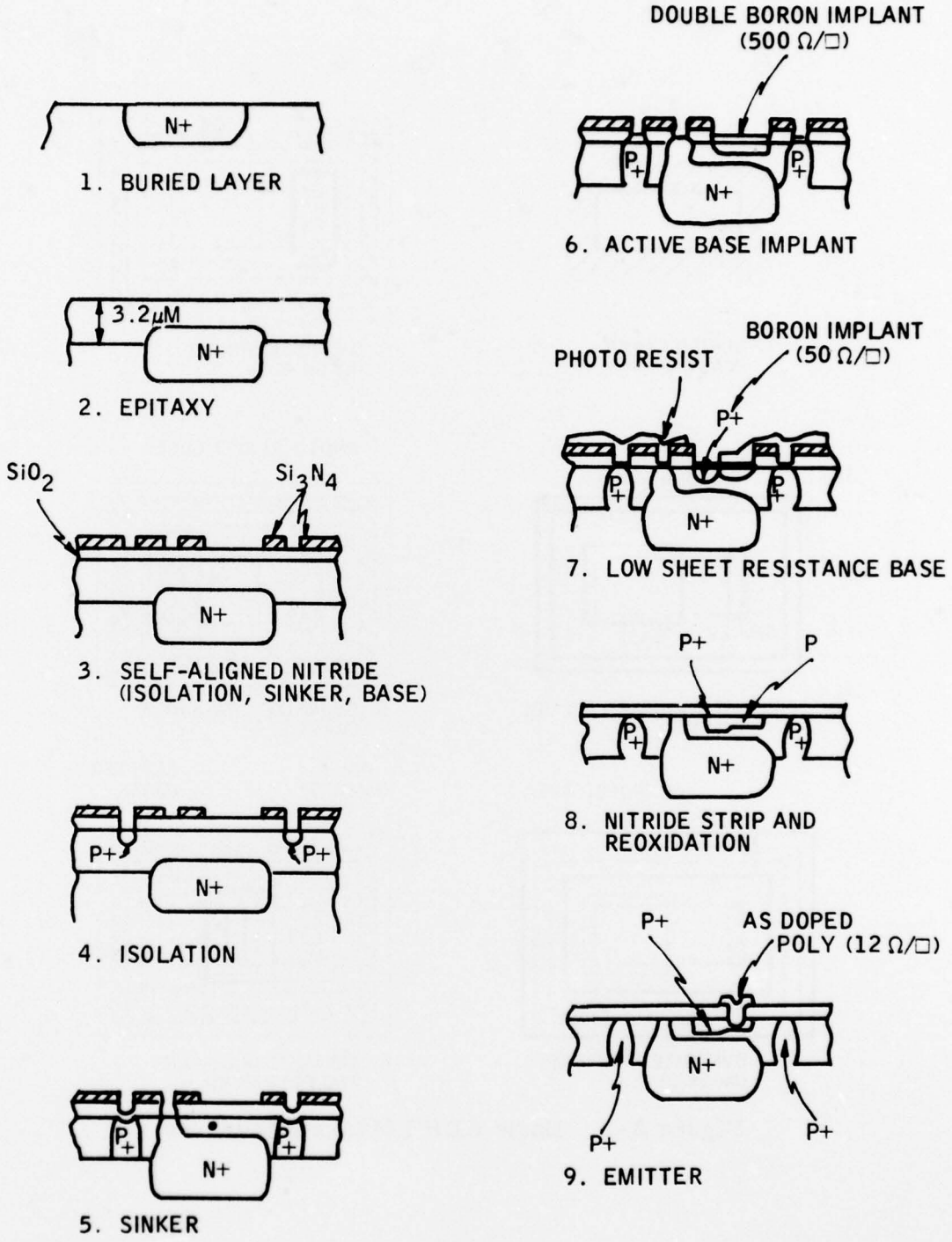


Figure A-1. Basic ABP I Processing Sequence

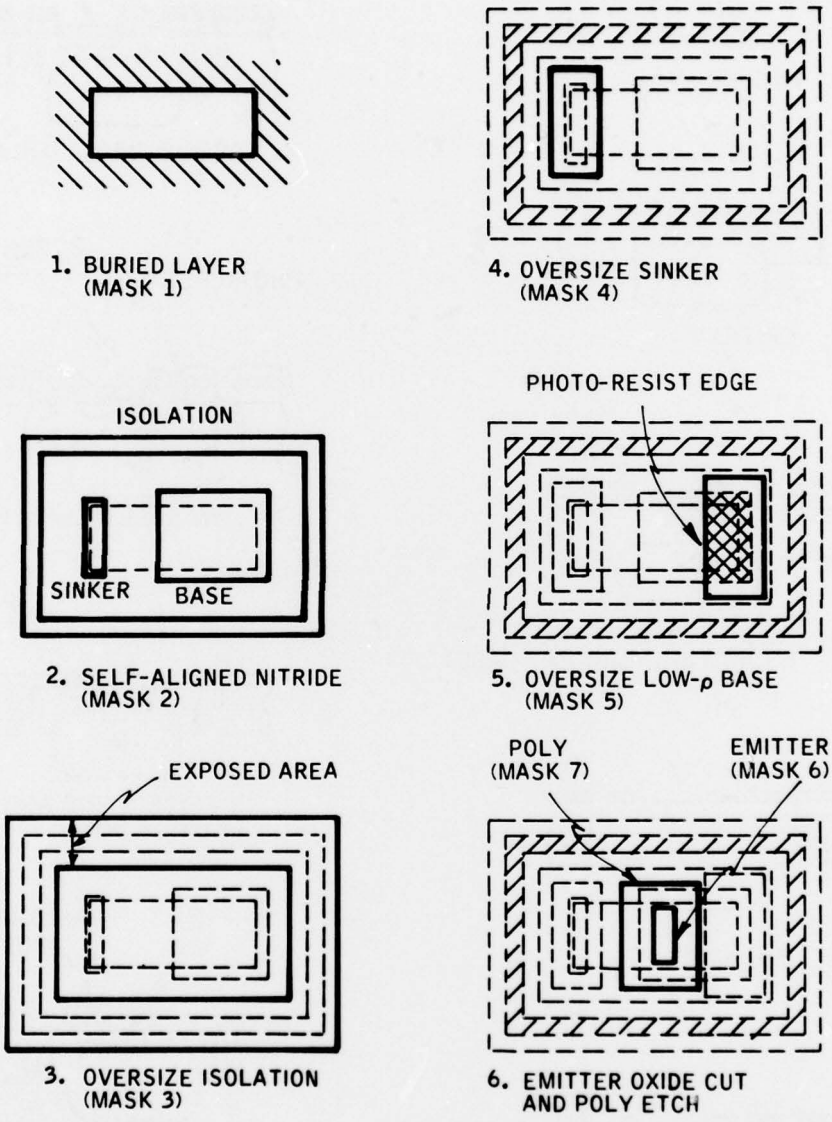


Figure A-2. Basic ABP I Masking Sequence

A thick SiO_2 layer is then grown over the nitride and the oversize isolation pattern (third mask, Figure A-2.3) is etched into it. This oversize mask technique allows very loose alignment tolerances. The object is to remove the oxide from the previously etched nitride opening for the isolation region only. The only constraint on the oversize mask registration is that it does not expose the base or sinker nitride cuts.

The heavily doped P^+ isolation region is then diffused into the epi layer (Figure A-1.4). A thin oxide layer is grown over the wafer, and, using the oversize sinker pattern (fourth mask, Figure A-2.4) in the same way the isolation pattern was used, the N^+ sinker is diffused into the epi layer until it contacts the buried layer. During this diffusion drive-in, the P^+ isolation diffuses through the epi and contacts the substrate (Figure A-1.5). For the base implants, all the oxide is etched off, exposing isolation and sinker, as well as the base nitride cuts. Ion implanting the P base into the P^+ isolation or the N^+ sinker does not change their profiles because the P base is very lightly doped relative to the P^+ and N^+ levels (Figure A-1.6). No mask is required for this step.

The next step (low-ρ base region) is ion-implanted using the photoresist pattern (fifth mask, Figure A-2.5) rather than an oxide pattern. Notice that the nitride base cut defines three edges of the low-ρ base, and the photoresist defines the fourth edge (Figure A-1.7). The nitride and oxide are then stripped off and a clean layer of oxide is grown on the wafer. During this oxide growth, the base region implants are partially annealed and the base profile in the epi layer is defined (Figure A-1.8). The emitter mask (Figure A-2.6) is used to etch the emitter pattern into this oxide. The emitter diffusion comes from the doped poly, which is deposited and then etched using the seventh mask (Figures A-1.9 and A-2.6). The remaining steps (contacts and metal) are not shown because they are standard processing steps well known to all semiconductor processing. Either single-metal or double-metal systems are available to be used to interconnect the various components diffused into the epi.

Some of the features that result from this processing sequence are:

- There is self-alignment through use of a silicon nitride cut that defines the field region. This feature allows for considerable simplification of the processing sequence, ultimately making the processing largely insensitive to photomask defects, etching errors, oxidation aberrations, etc. One further advantage of this technique is the ability of the nitride to ensure proper shielding of the field regions from the base implants.

- The base region is composed of a three-part boron implantation. This allows for the possibility of producing two independently adjustable base resistors. The key feature here is the use of a double-boron implant for the active transistor region (a deep implant for active characteristics, and a shallow one for sheet resistance purposes), and a heavier implant for a low-resistance inactive base (used to reduce r_b'). This arrangement allows the inactive base sheet resistance to be varied from 35 to 130 $\Omega/\square$, and the active base resistance to be varied from 350 to 1000 $\Omega/\square$.

- Photoresist shielding is used during the inactive base implant and greatly simplifies the processing by allowing for the use of only one implant oxidation.

- A polysilicon, arsenic-doped emitter allows for the elimination of the aluminum spiking problem inherent in shallow emitter structures. Also, by maintaining the emitter concentration at a high level ($10^{20}/cm^3$), advantage is taken of the concentration-enhanced diffusivity of arsenic to produce a narrow base region with a steep emitter-base profile. This

allows for better emitter efficiency, while maintaining the base push effect of phosphorous.

Figure A-3 gives the emitter-base-collector diffusion profile produced by this process. Notice the steep emitter doping gradient (for efficient injection), the relatively narrow base (for high-frequency response), and the

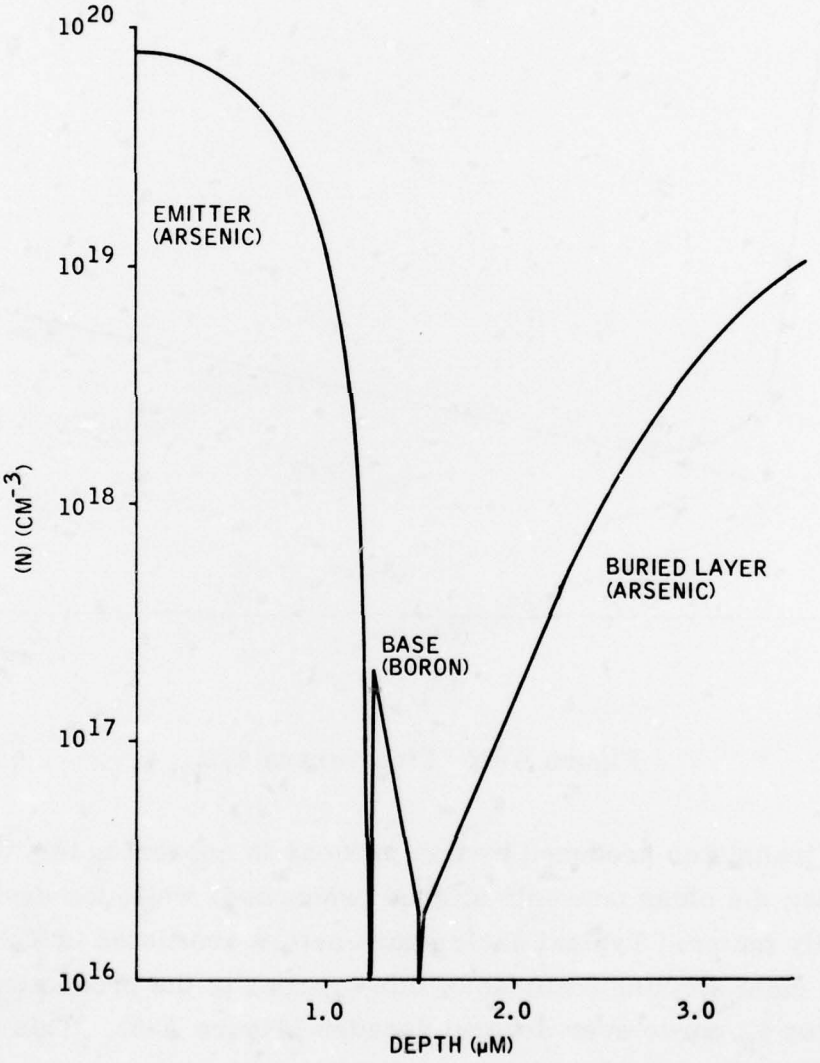


Figure A-3. The Emitter-Base Buried-Layer Doping Profile as Found From Spreading Resistance Measurements

proximity of the buried layer (for low saturation resistance). The intrinsic transit time of the base region is about 300 ps, as shown by the plot of $1/I_E$ versus $1/f_T$ (Figure A-4).

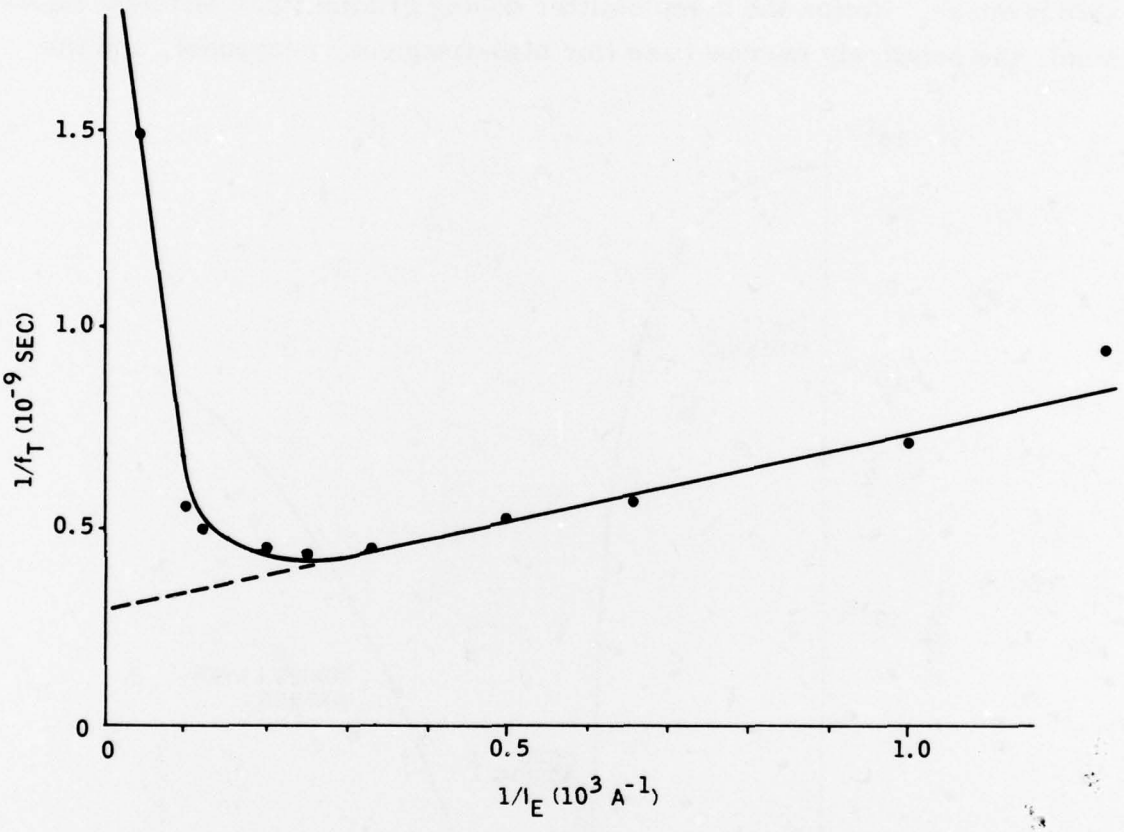


Figure A-4. $1/f_T$ versus $1/I_E$

The basic transistor produced by this process is approximately 60 percent smaller than the older non-self-aligned processes, while the devices are intrinsically faster. Typical device parameters are listed in Table A-1. One of the most striking features of this process is the production of a flat β versus I_E curve over several decades (Figure A-5). This feature is due to a general predominance of the diffusion current over the recombination current at all current levels greater than 10^{-10} A.

TABLE A-1. TYPICAL DEVICE PARAMETERS

Parameter	Value	Units
H_{fe}	80	
f_T	2.1	GHz
R_{SAT}	10	Ω
R_b'	190	Ω
BV_{bco}	25	V
I_{cbo} at 3 V reverse bias	$<10^{-10}$	A
BV_{beo}	5.6	V
BV_{ceo}	11	V
C_{be} at 0 V	0.45	pF
C_{bc} at 0 V	0.55	pF
R_E	5	Ω
Emitter-base I-V slope	60	mV/decade

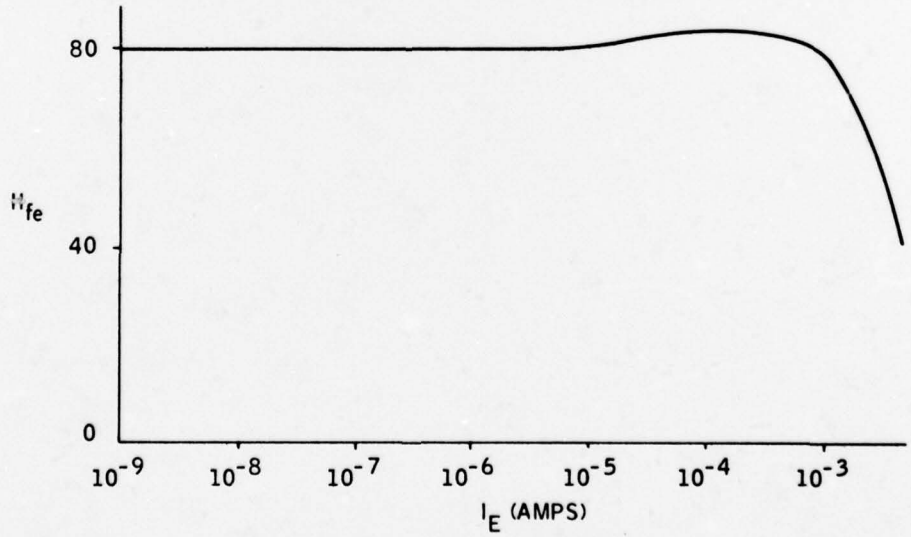


Figure A-5. H_{fe} versus I_E

APPENDIX B

PULSE JITTER DUE TO NOISE

APPENDIX B

PULSE JITTER DUE TO NOISE

For BER = 10^{-8}

$$\frac{i_s}{I_n} = 5.62 \qquad i_s = \frac{Is}{2}$$

$$\frac{I_s}{i_n} = 11.24$$

For a receiver transresistance of R_T the voltages at the comparitor input are:

$$E_S = R_T I_S \text{ and } e_n = R_T i_n \text{ (rms) or } 1\sigma \text{ limit}$$

Thus, the voltage S/N at the comparitor input is:

$$S/N = \frac{I_S R_T}{i_n R_T} = \frac{E_s}{e_n} = 11.24$$

The noise bandwidth of the receiver is only slightly more than the signal bandwidth. Therefore, the noise voltage contains the same frequency components as the signal voltage. In any case, the bandwidth of the comparitor can be limited if necessary so that it will not respond to short noise pulses.

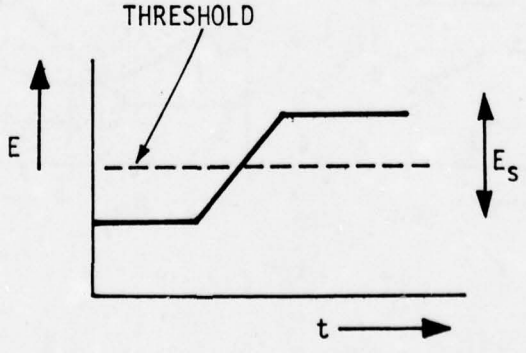
The minimum slew rate of E_s occurs when the LED has t_0 = 15 ns (10 percent to 90 percent) and $I_s = I_S$ min = 250 nA. For a worst case receiver bandwidth of 10 MHz, the receiver rise time is t_R = 0.35/10 MHz = 35 ns and the total composite rise time of E_s is

$$t_T = (35^2 + 15^2)^{\frac{1}{2}} = 38 \text{ ns}$$

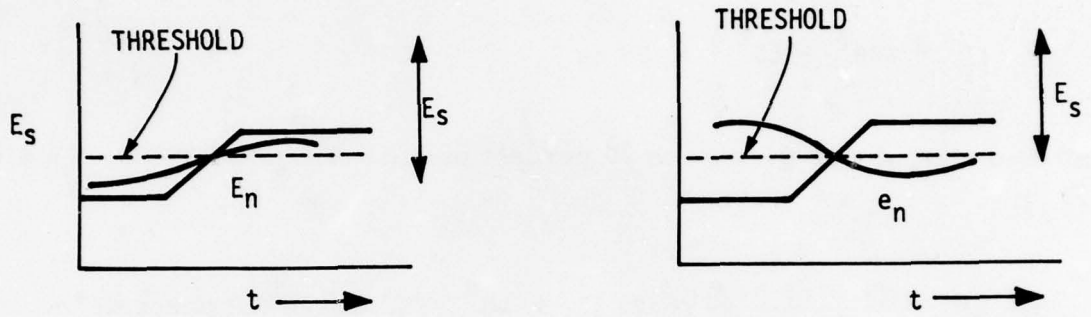
Approximating the 10 percent to 90 percent portion of E_s as a ramp, the slew rate is:

$$SR = \frac{(0.8)Es \text{ min}}{38 \text{ ns}} = 21 E_s \times 10^6 \text{ V/S, where (10 percent to 90 percent) = 0.8}$$

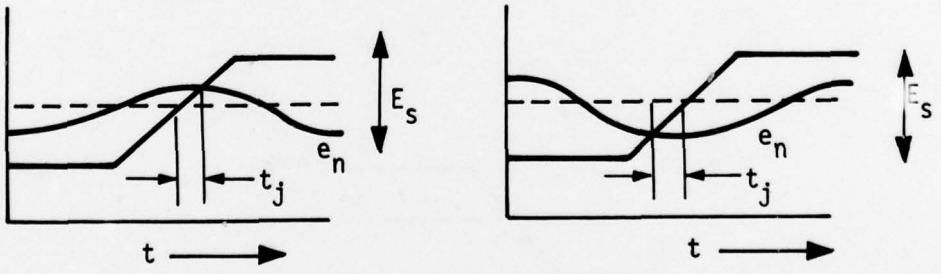
If $e_n = 0$ the comparator circuit will threshold the output signal voltage at $E_s/2$ for all values of E_s.



When a noise voltage is present, it can have arbitrary phase with the signal. If e_n is in phase or 180 degrees out of phase with E_s, then the threshold crossing is not shifted.



If, on the other hand, e_n is $\pm$90 degrees phase to E_s, there is a shift in the zero crossing. Assume the noise voltage shifts the threshold.



The peak value of the jitter of the threshold crossing for each value of noise voltage E_n is

$$T_j = \frac{E_n}{S_R} = \frac{E_n V}{E_s(21 \times 10^6 \text{ V/s})}$$

$$T_j = \frac{E_n}{E_s} \; 47.5 \text{ ns}$$

Since the phase of the noise is arbitrary with respect to E_s with a uniform probability of any given phase, it follows that the rms jitter for each amplitude E_n is given by

$$t_J = \frac{E_n}{2E_s} \; 47.5 \text{ ns} = \frac{E_n}{E_s} \; 33.6 \text{ ns}$$

The values of E_n form a standard Gaussian bell-shaped distribution (all thermal noise and shot noise sources). Therefore, the total rms value of jitter sampled in time over all phases and all values of E_n is

Therefore, the total rms value of jitter sampled in time over all phases and all values of E_n is

$$T_j = \frac{e_n}{E_s} \; 33.6 \text{ ns, but } \frac{E_s}{e_n} = 11.24 \text{ for BER} = 10^{-8}$$

Thus, it follows that the rms jitter of the received signal is

$$(\text{rms})\ t_j = \frac{33.6\ \text{ns}}{11.24} = 3\ \text{ns}$$

$$t_j = 3\ \text{ns} \qquad \text{for BER} = 10^{-8}$$

For any increase in E_s over the minimum or any value of e_n < the specified value, the jitter will decrease. Thus, the jitter will always be worst case at the minimum input signal and drop as the signal increases.